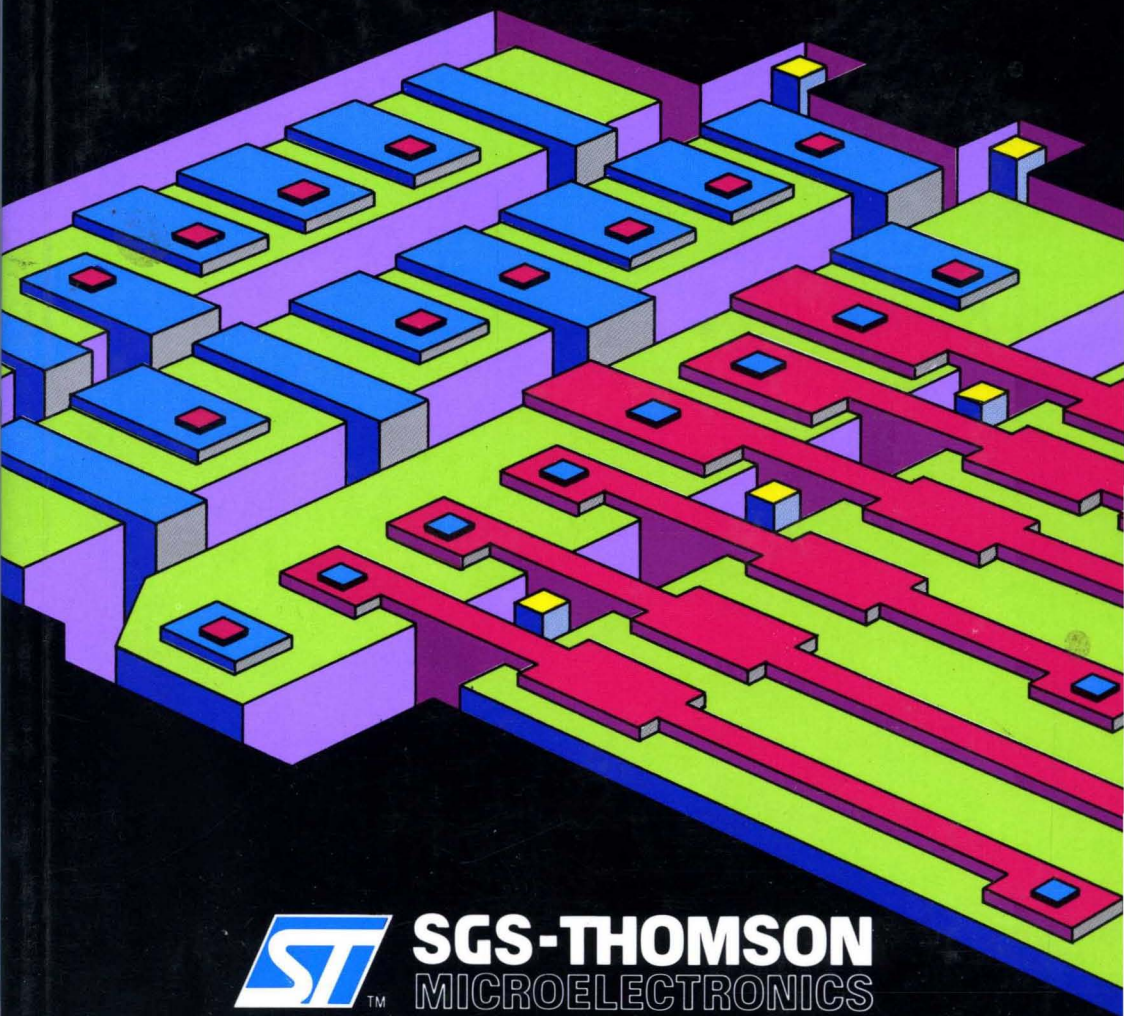


# GRAPHIC PROCESSORS

DATABOOK

1<sup>st</sup> EDITION



**SGS-THOMSON**  
MICROELECTRONICS









---

# GENERAL INDEX

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# **PRODUCT GUIDE**







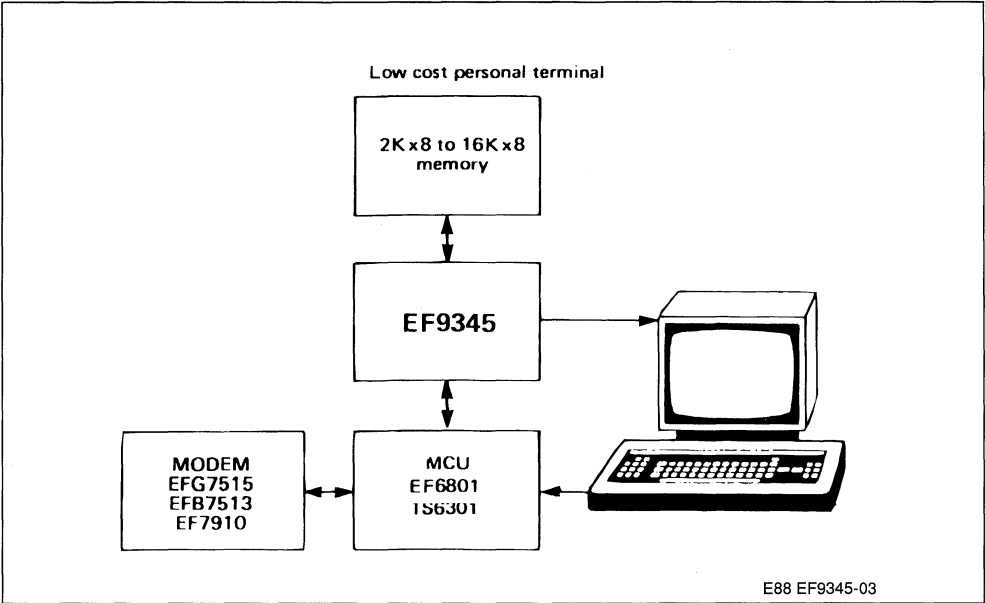


# **ALPHANUMERIC and SEMI-GRAPHIC CRT CONTROLLERS**

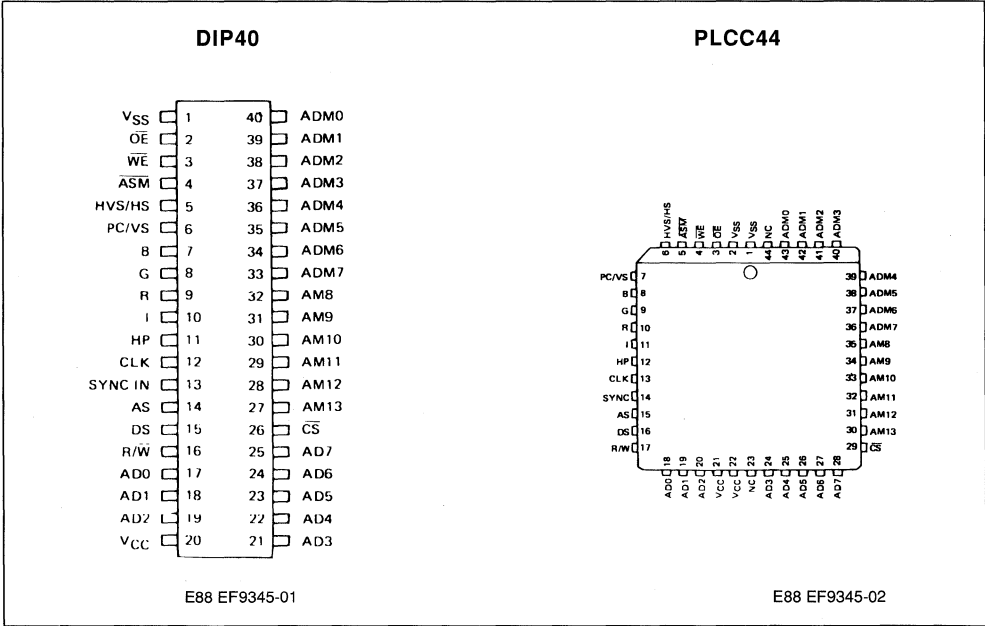




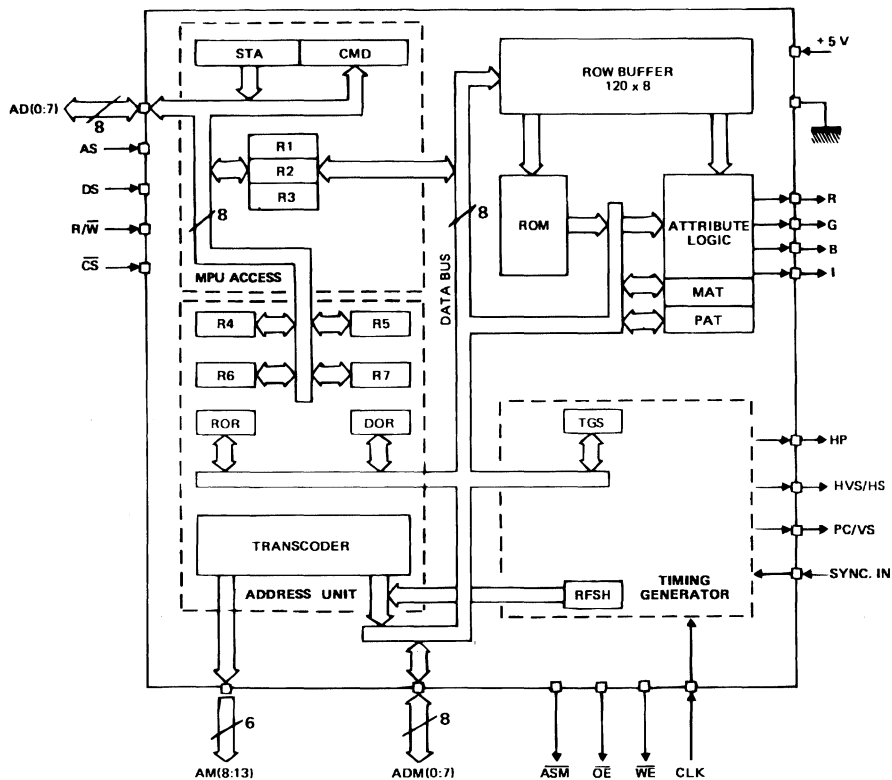
TYPICAL APPLICATION



PIN CONNECTION



## BLOCK DIAGRAM



E88 EF9345-04









































Figure 7 : Coloring with Quadrichrome Characters.

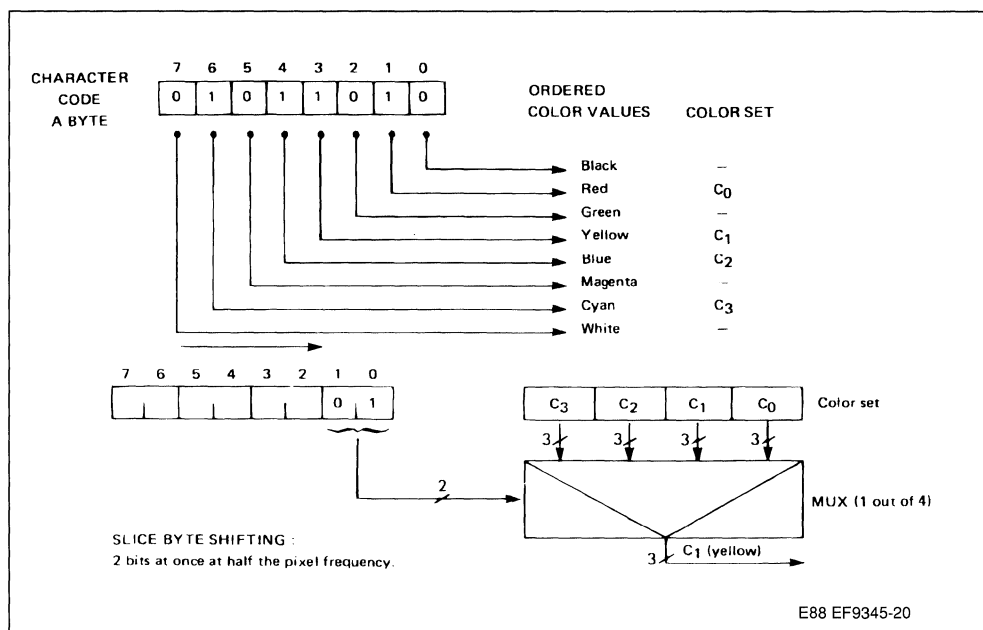


Figure 8 : Fixed Long Codes in Memory 120 Byte Row Buffer.

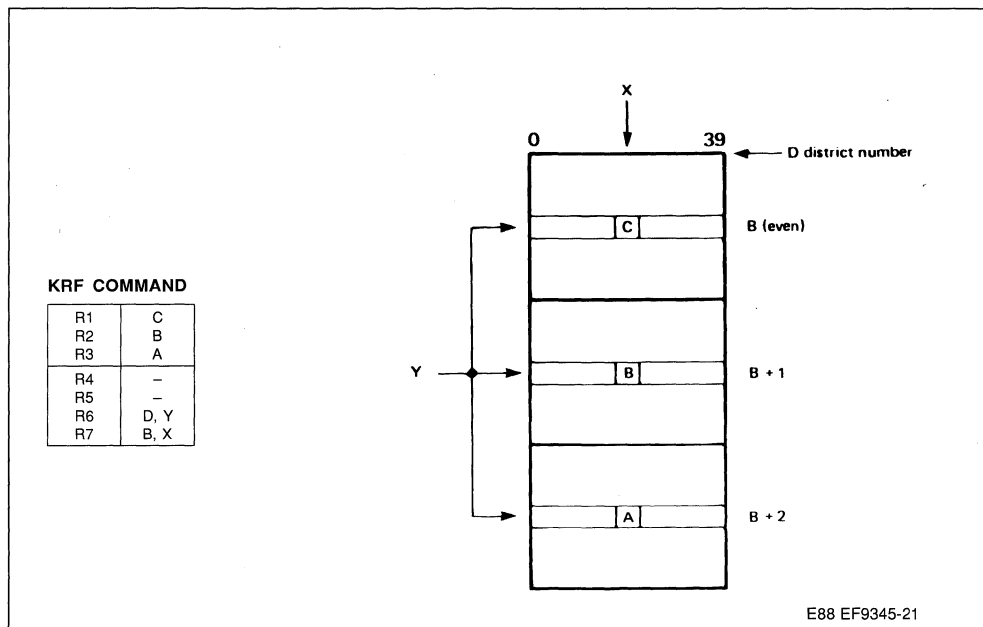




































Figure 21 : 80 Char/Row Code Packing.

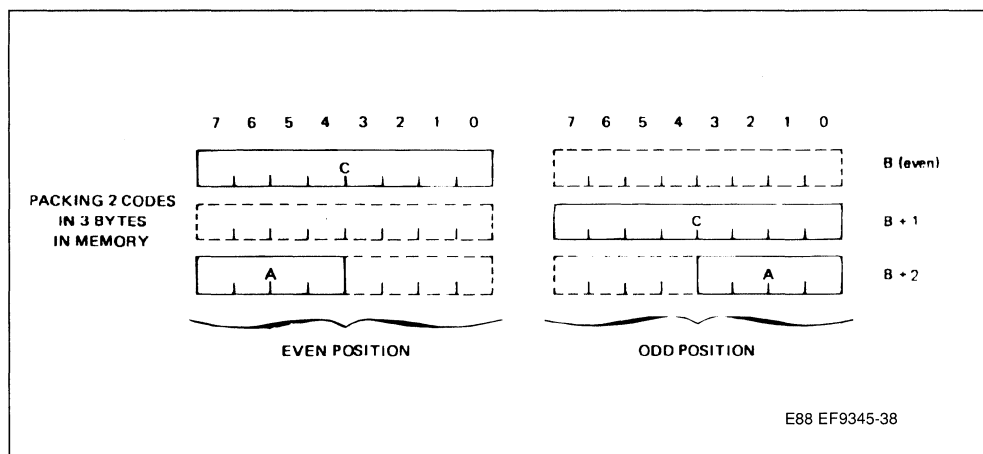
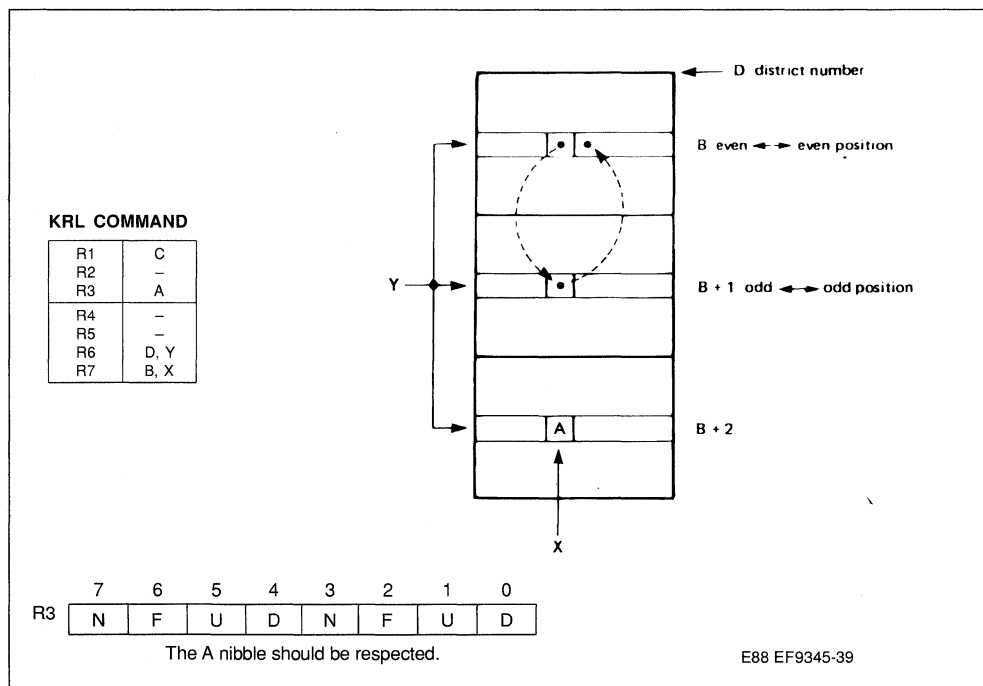


Figure 22 : KRL Command : Sequential Access to Long Codes.















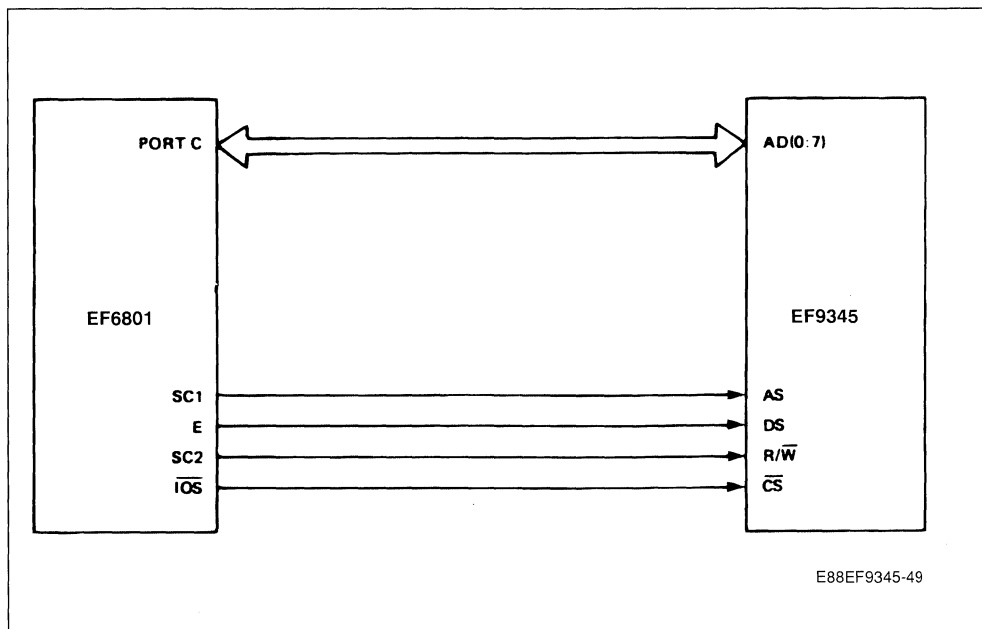






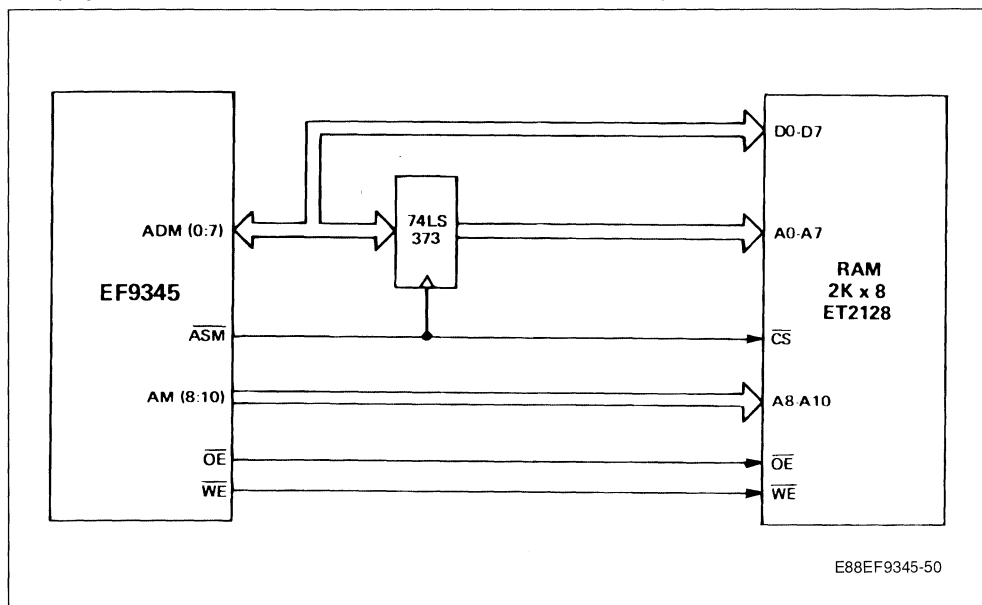


## INTERFACE WITH EF6801



## MINIMUM APPLICATION WITH 2K X 8 MEMORY

One page memory terminal in 16-bit fixed format or 24-bit compressed format.



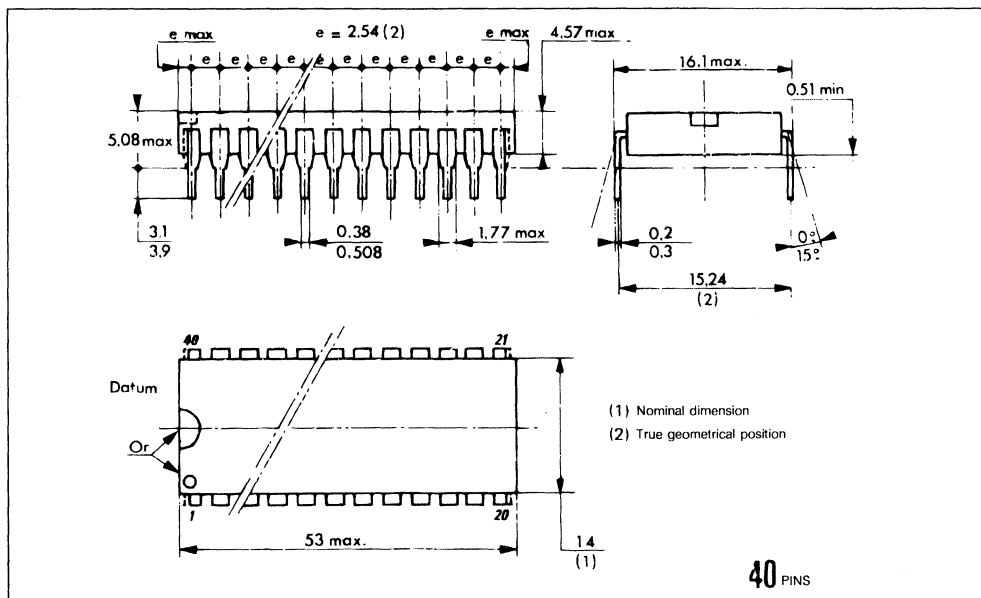


## ORDERING INFORMATION

Part Number	Package	Character Generator
EF9345PRYYY	DIP40	RYYY
EF9345FNYYY	PLCC44	RYYY

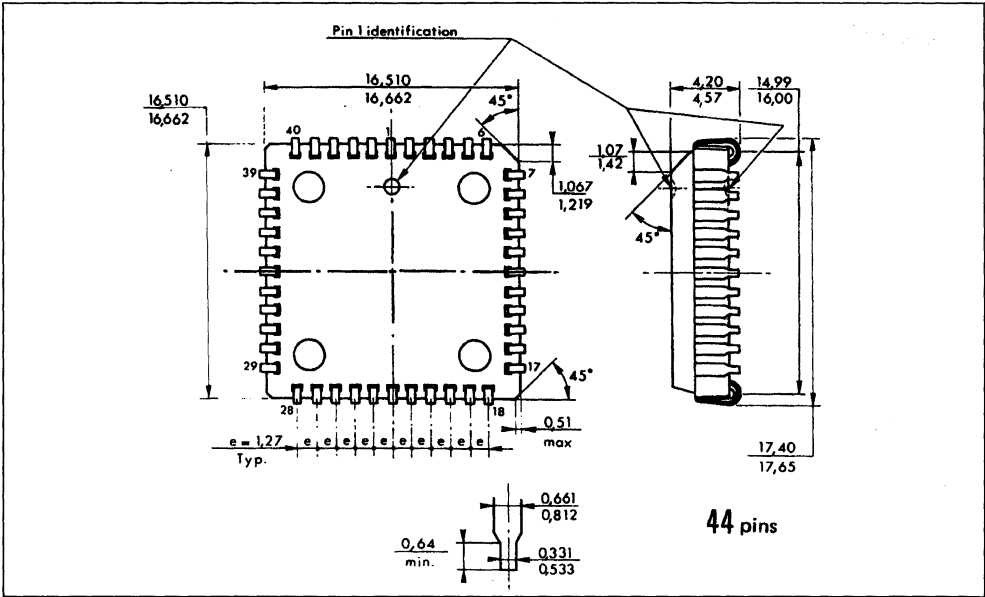
## PACKAGE MECHANICAL DATA

40 PINS – PLASTIC DIP



PACKAGE MECHANICAL DATA (continued)

44 PINS – PLASTIC CHIP CARRIER

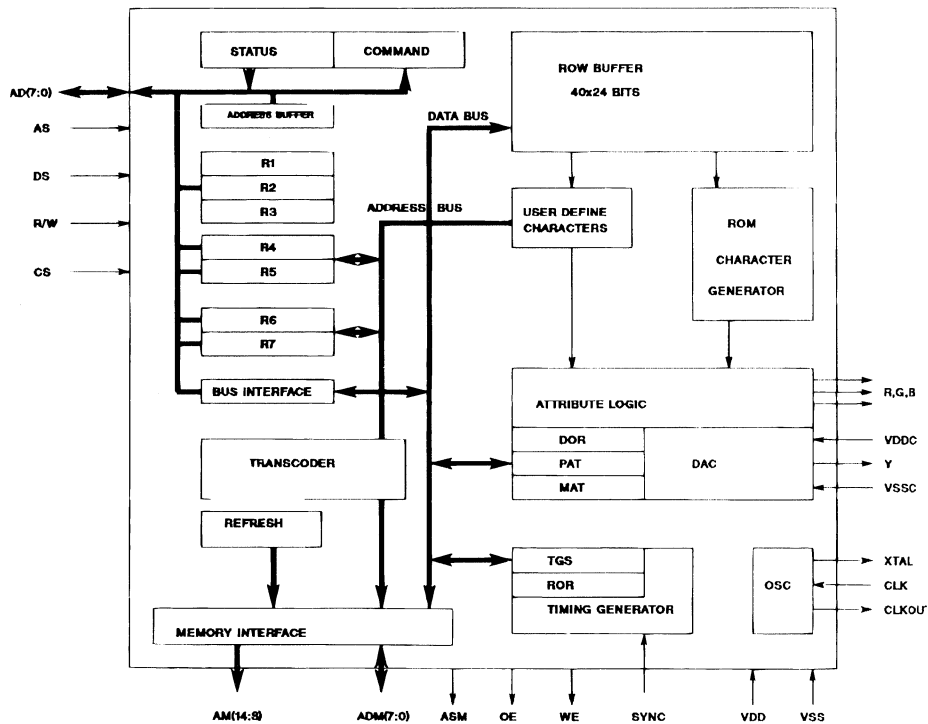








## BLOCK DIAGRAM



E88TS9347-02

























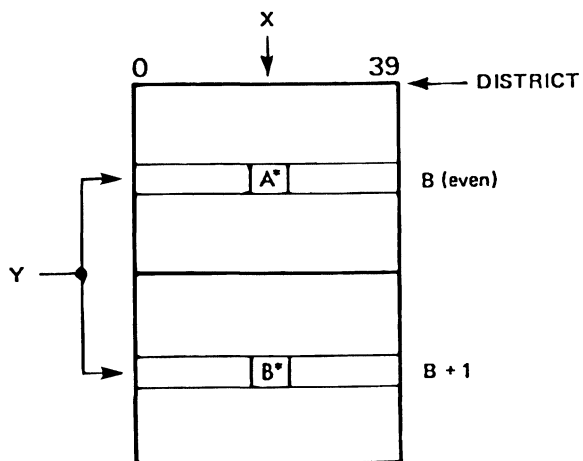
Figure 9 : Short Codes in Memory Double Row Buffer.

**TSM COMMAND**

R1	A*
R2	B*
R3	W
R4	—
R5	—
R6	D, Y
R7	B, X

**TSA COMMAND**

R1	A*
R2	B*
R3	W
R4	D, Y
R5	B, X
R6	
R7	



E88TS9347-12



















Figure 19 : KRL Command : Sequential Access to Long Codes.

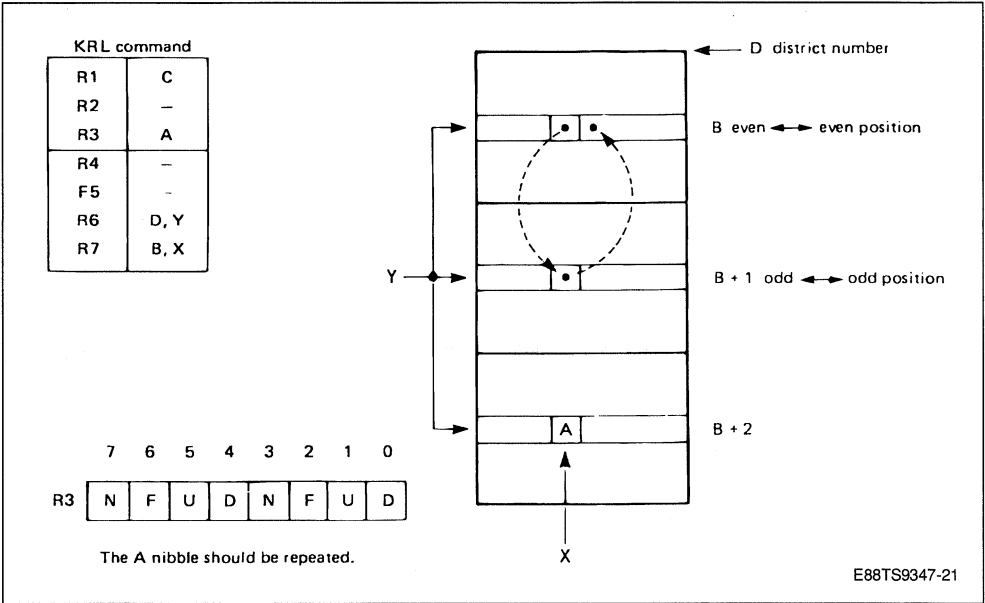
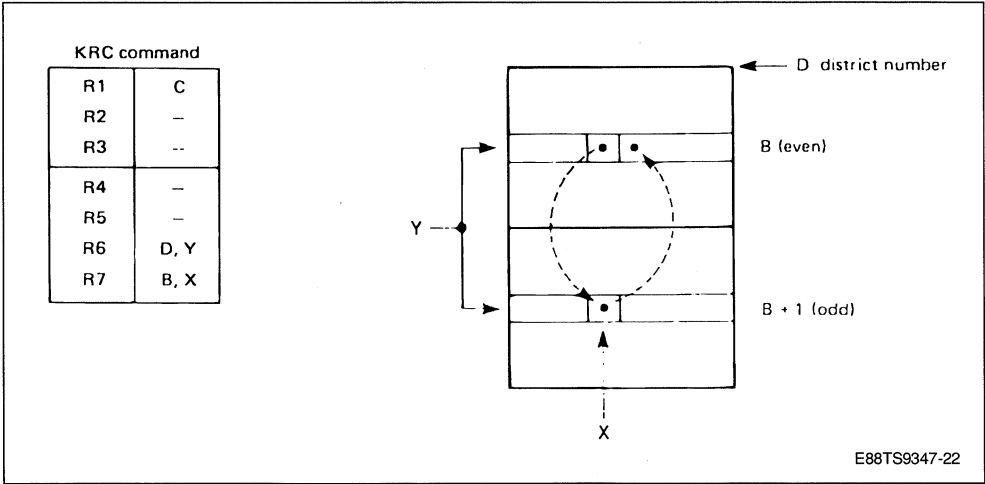


Figure 20 : KRS Command Sequential Access to Short Codes.







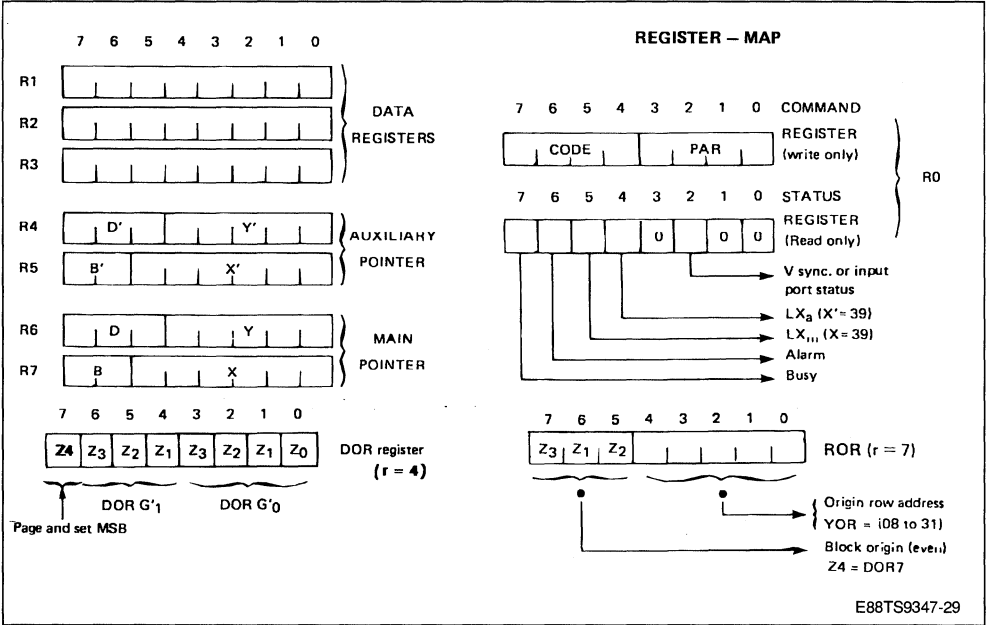








REGISTER – MAP





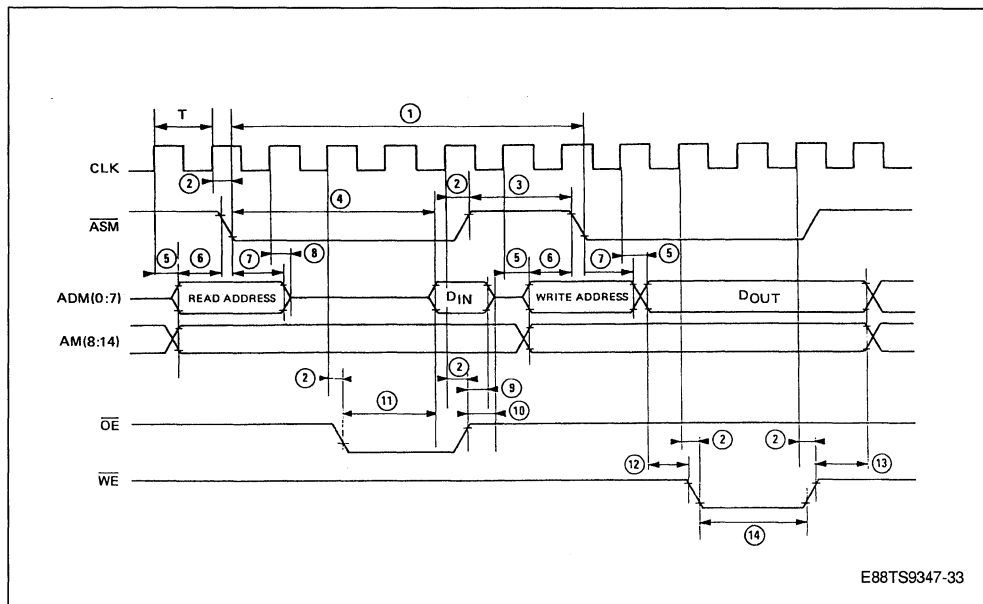








## MEMORY INTERFACE TIMING DIAGRAM











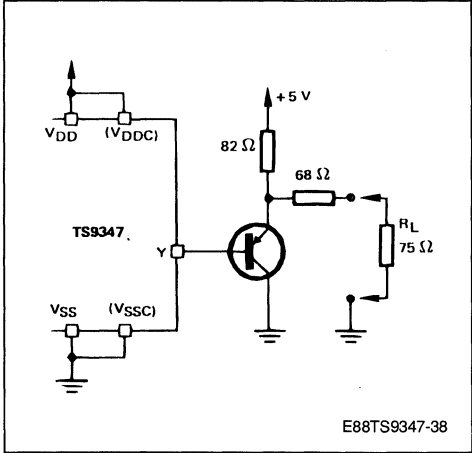
ELECTRICAL SPECIFICATION

Over Full Temperature Range :  $V_{DDC} = V_{DD} = 5\text{ V}$  (see note 1)  
 $V_{SSC} = V_{SS} = 0\text{ V}$  ;  $C_L = 20\text{ pF}$ ,  $R_L > 100\text{ K}$  to  $V_{SS}$  or  $V_{DD}$

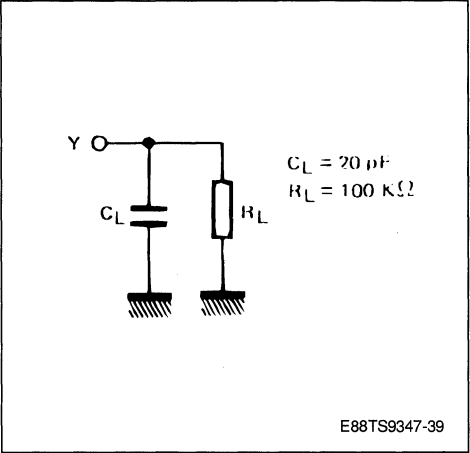
Parameter	Min.	Typ.	Max.	Unit
Monotonicity	Guaranteed			
Output Level Dispersion	-	10	50	mV
Propagation Delay (clock edge to 50 % output)	-	-	60	ns
Rise and Fall Time (10 – 90 %)	-	-	30	ns
Output Static Impedance	-	-	600	$\Omega$

Note : 1. The DAC is a 9 output potentiometric divider : therefore, each voltage variation on  $V_{DDC}$  is repercutated on the output with the same relative value with respect to  $V_{SSC}$ .

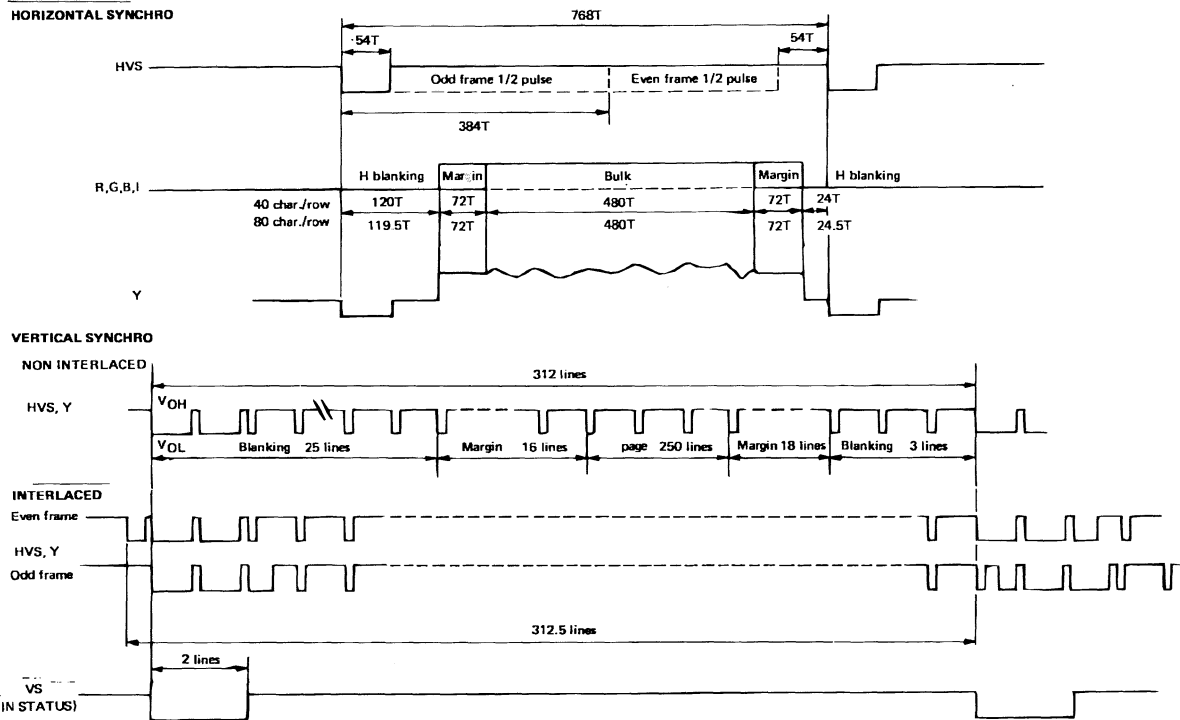
TYPICAL APPLICATION



TEST CONDITION



# VERTICAL AND HORIZONTAL SYNCHRONIZATION OUTPUTS ( $T_{clk}$ )



E88TS9347-40



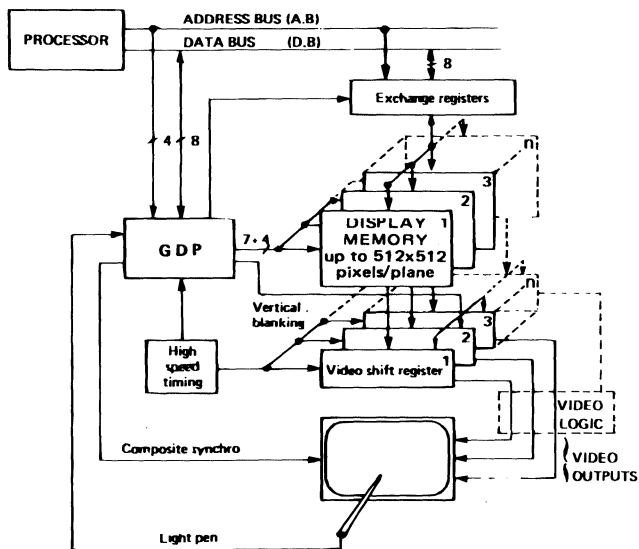


# **GRAPHICS CONTROLLERS**



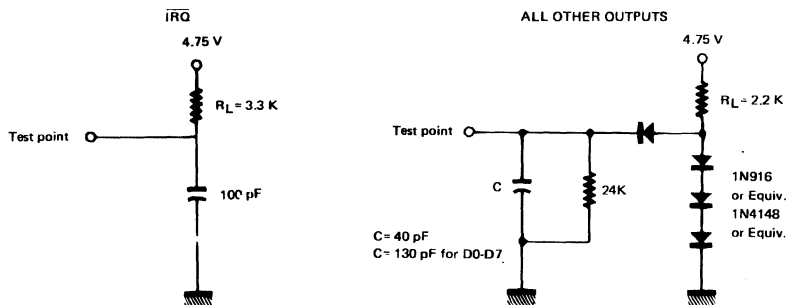


## TYPICAL APPLICATION



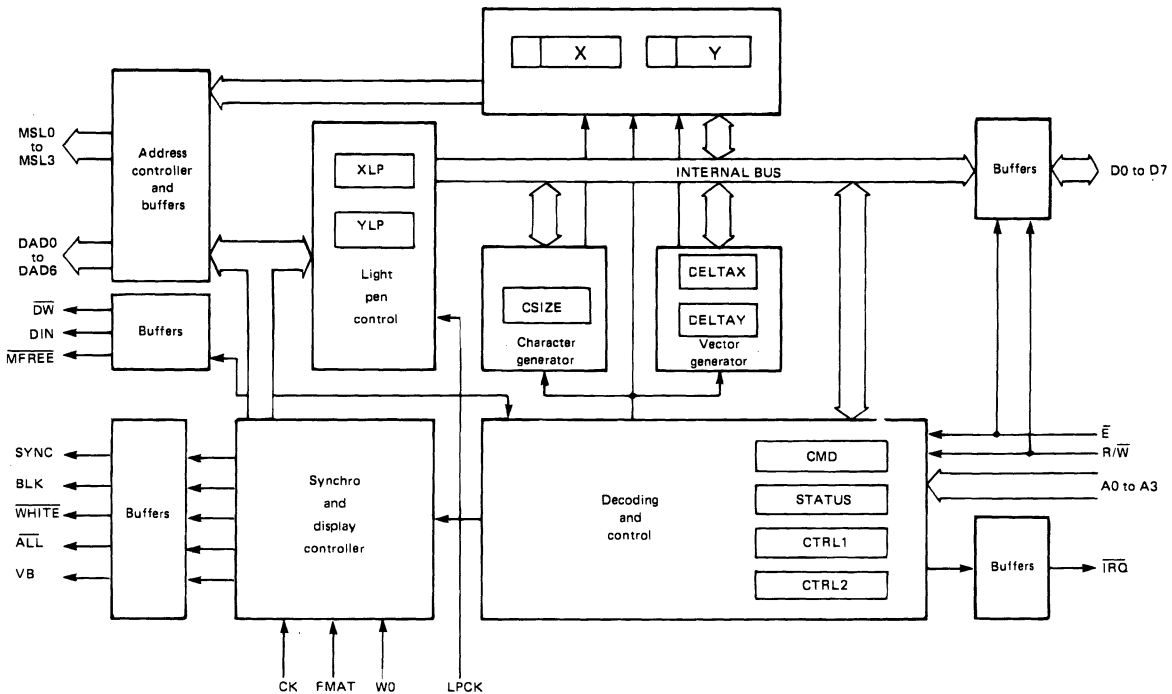
E88 EF9365-02

## TEST LOADS



E88 EF9365-04

BLOCK DIAGRAM



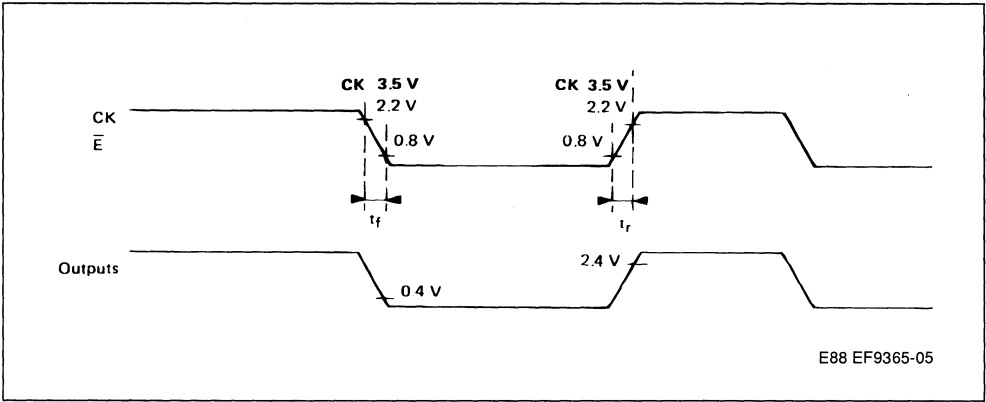
E88 EF9365-03



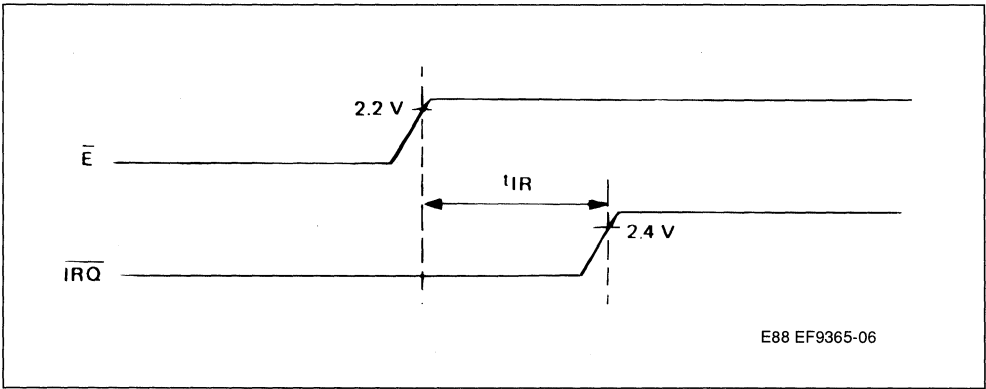




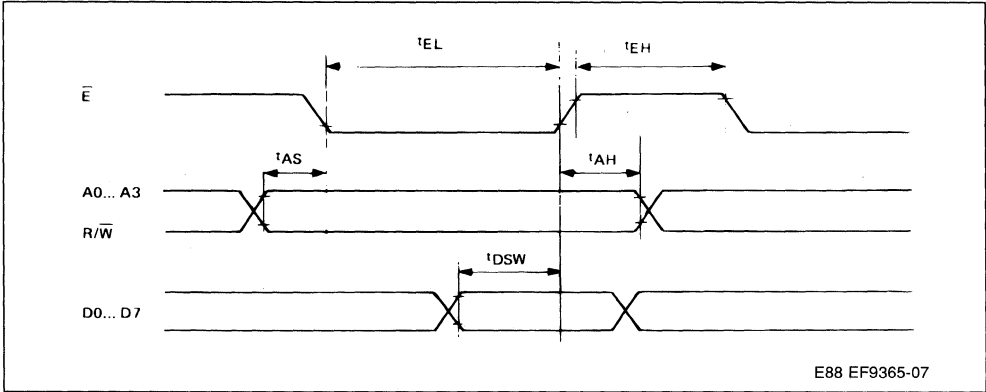
CLOCK AND OUTPUT CHARACTERISTICS



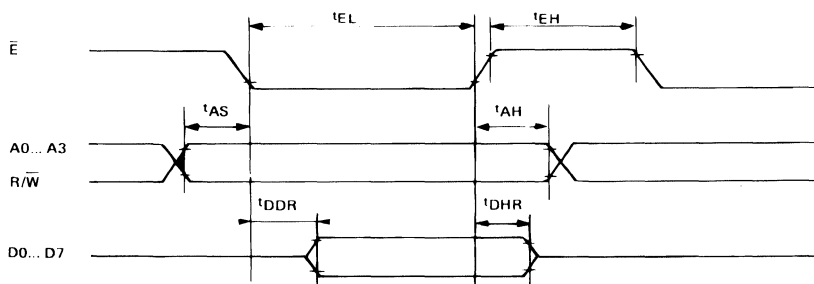
IRQ RELEASE TIME



MICROPROCESSOR BUS, WRITE ACCES

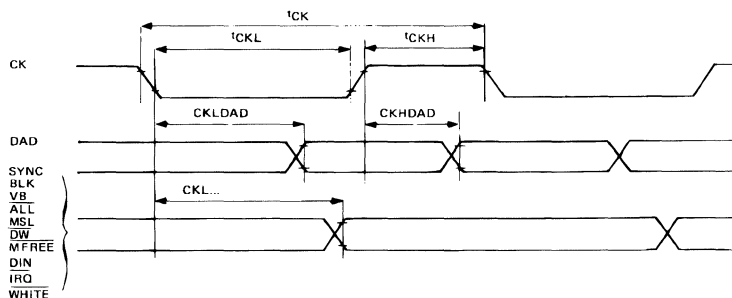


## MICROPROCESSOR BUS, READ ACCESS



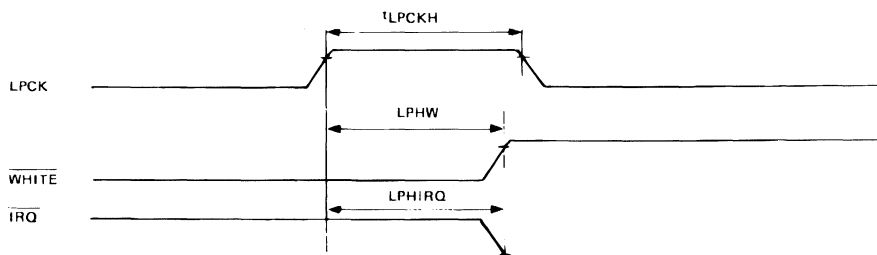
E88 EF9365-08

## SYNCHRONOUS SIGNALS WITH CK INPUT



E88 EF9365-09

## LIGHT PEN SIGNALS



E88 EF9365-10







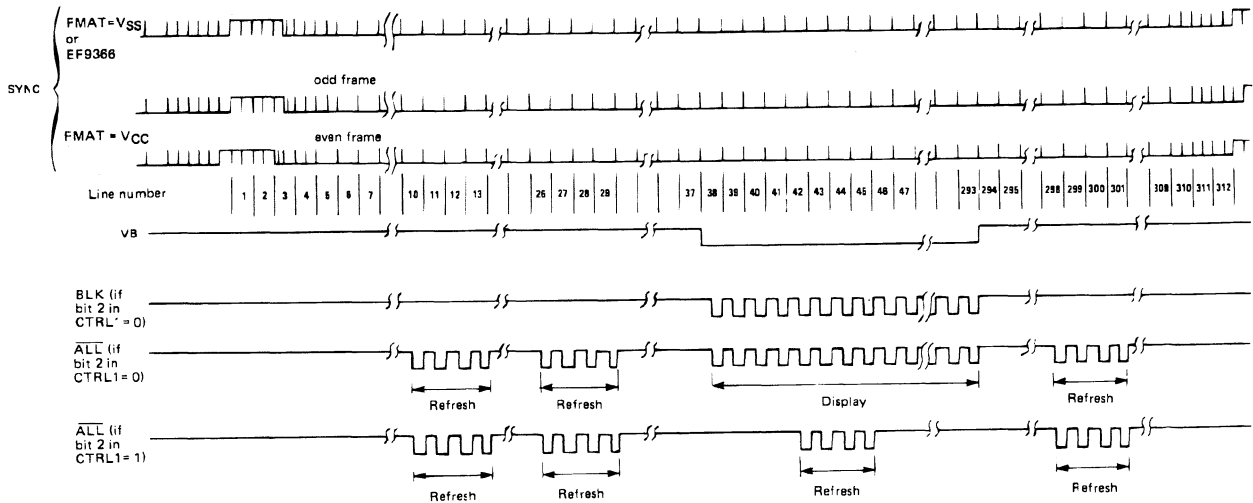








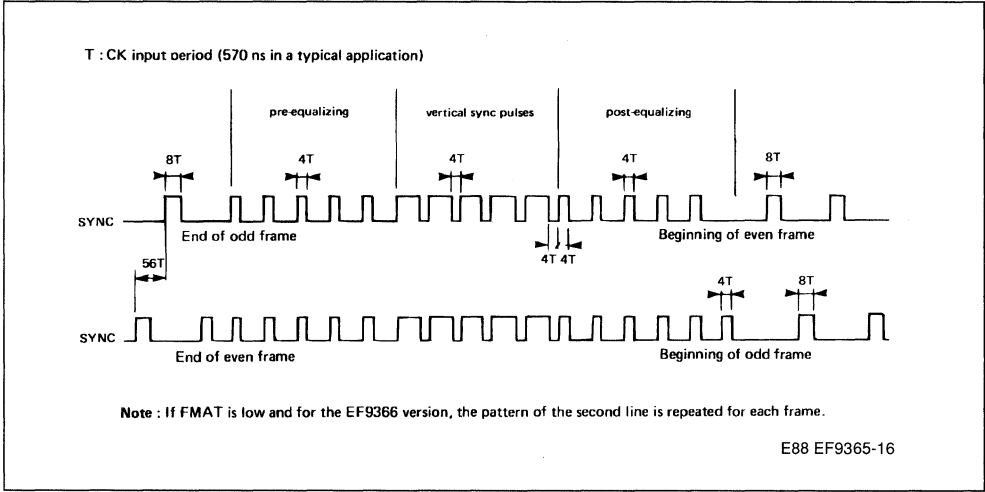




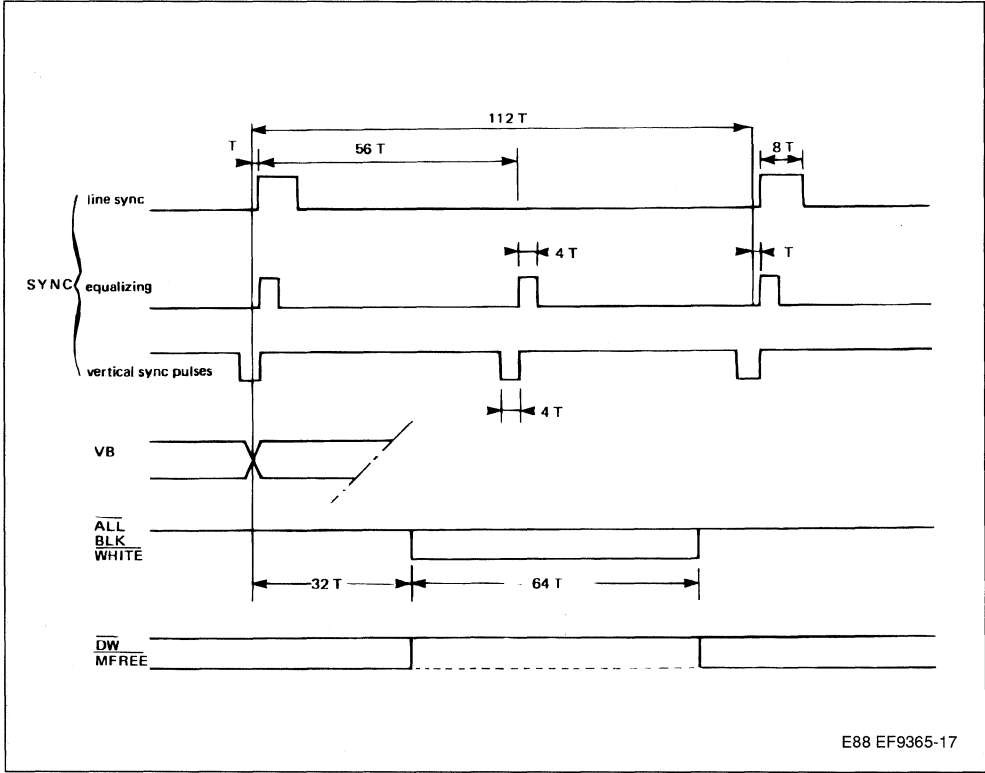
Note : ALL signal high denotes write periods.

E88 EF9365-15

COMPOSITE SYNC AROUND FRAME SYNC



DETAILED LINE DIAGRAM















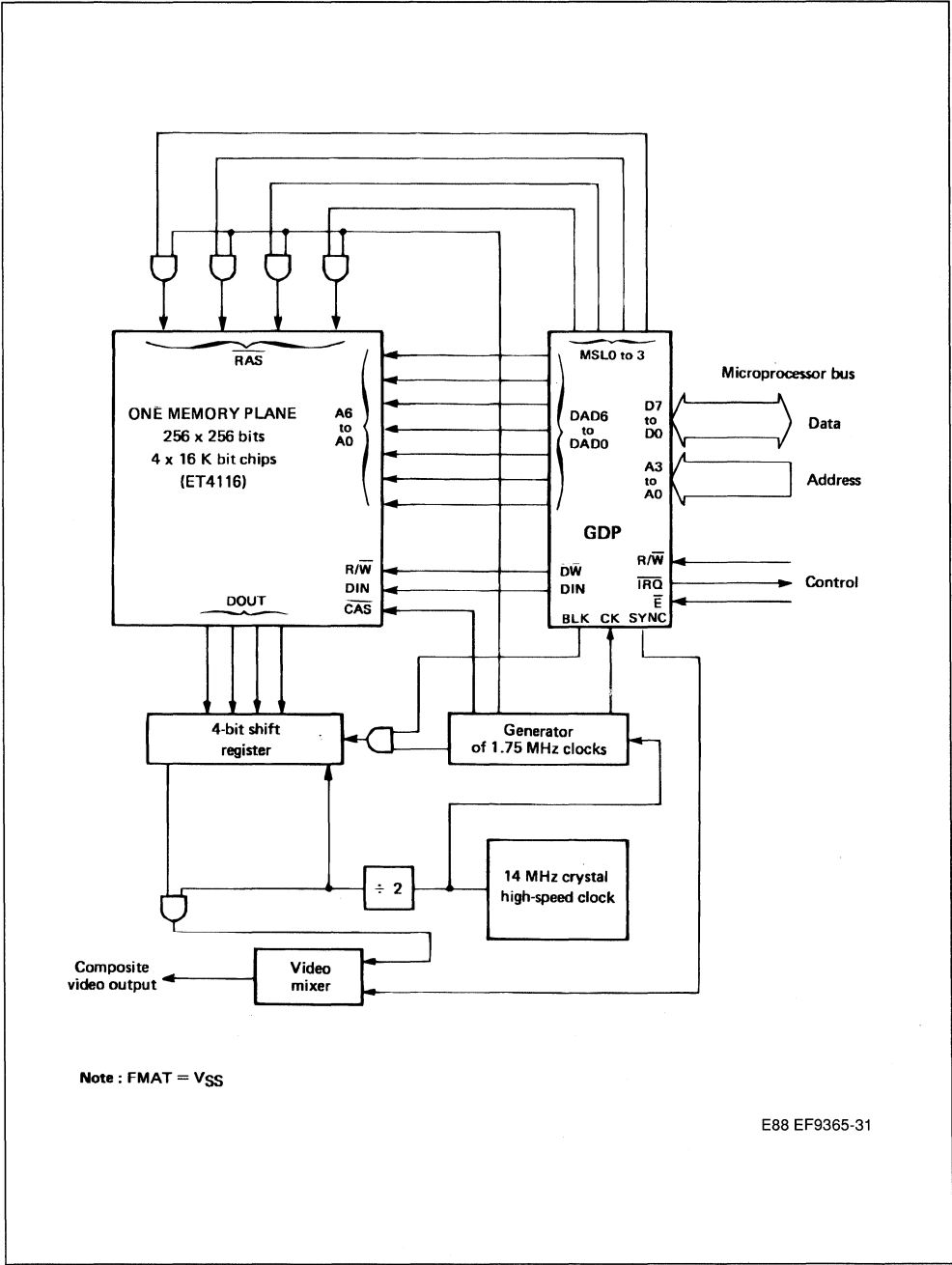








EXAMPLE OF AN APPLICATION OF THE EF9365 : 256 x 256 BLACK AND WHITE



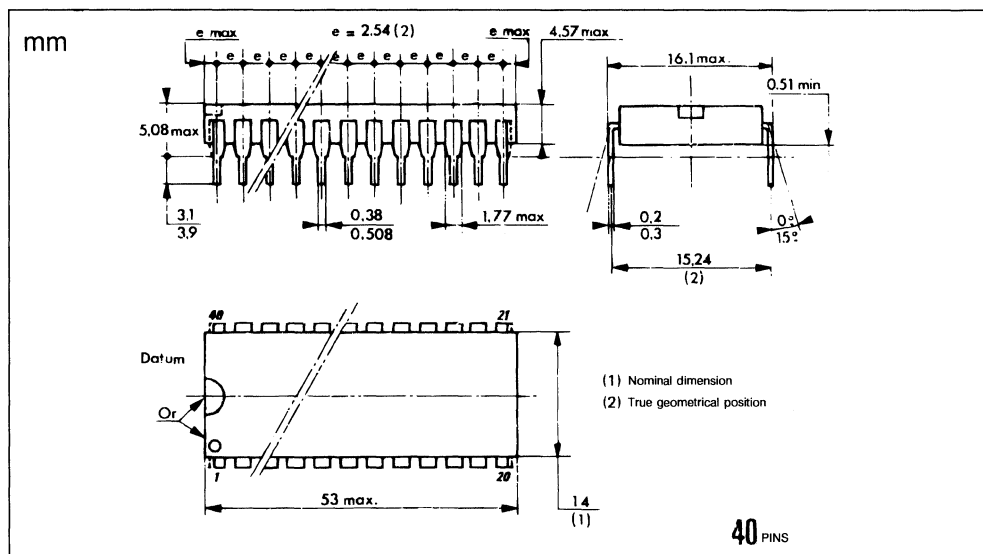
E88 EF9365-31





## PACKAGE MECHANICAL DATA

40 PINS - PLASTIC DIP



## ORDERING INFORMATION

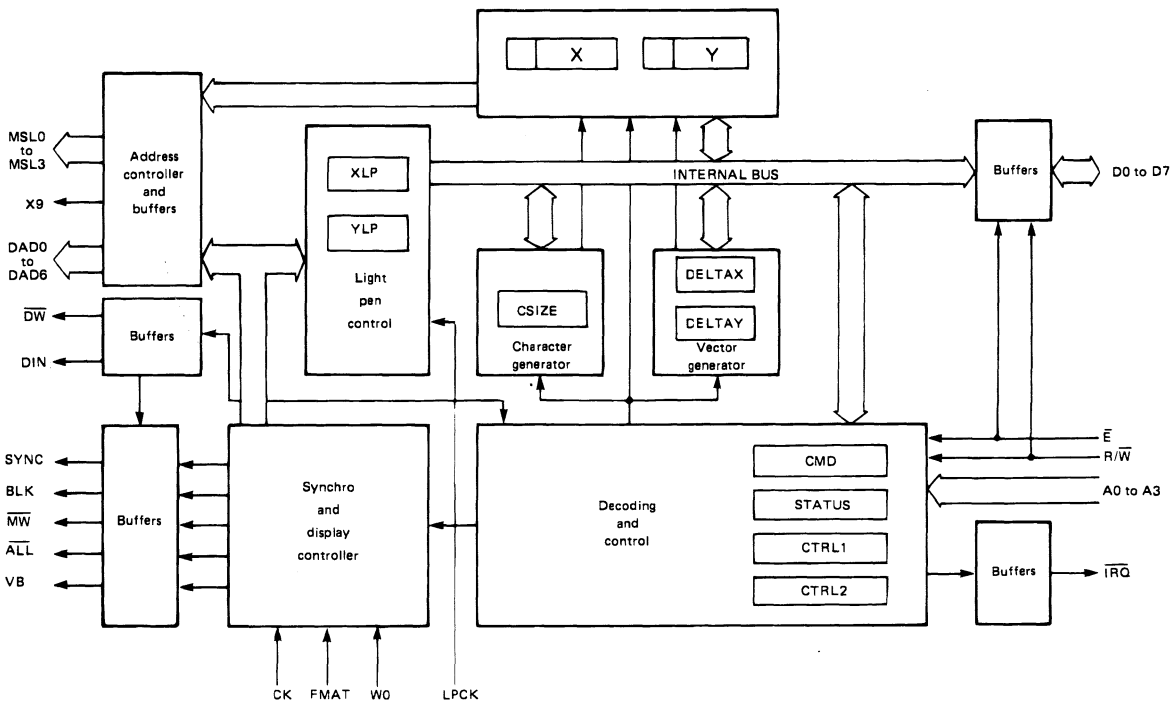
Part Number	Temperature Range	Package
EF9365P	0 to 70 °C	DIP 40
EF9366P	0 to 70 °C	DIP 40









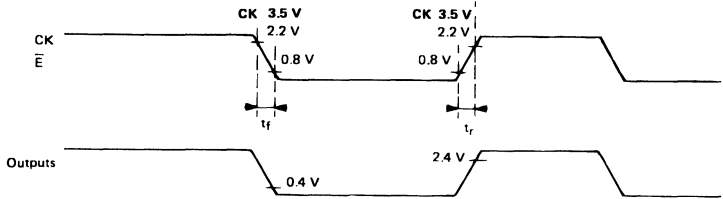


E88 EF9367-03



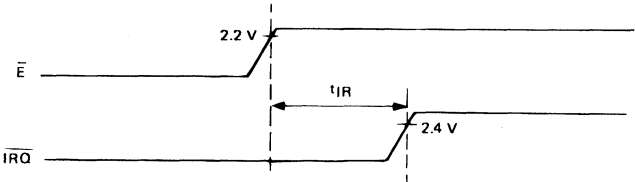


CLOCK AND OUTPUT CHARACTERISTICS



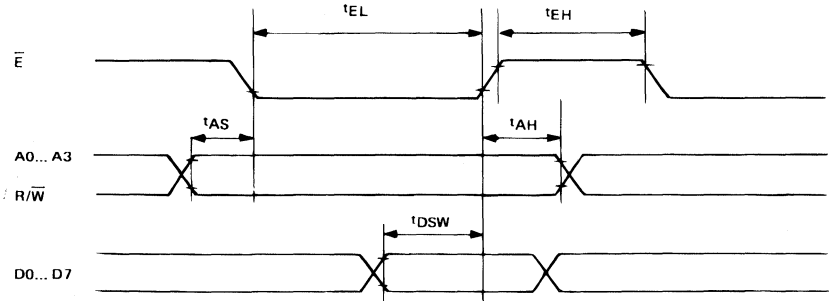
E88 EF9365-05

$\overline{IRQ}$  RELEASE TIME



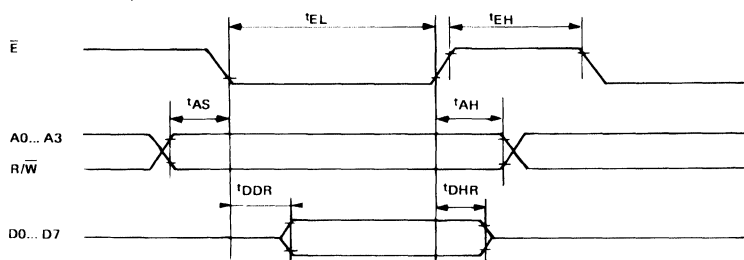
E88 EF9365-06

MICROPROCESSOR BUS, WRITE ACCESS



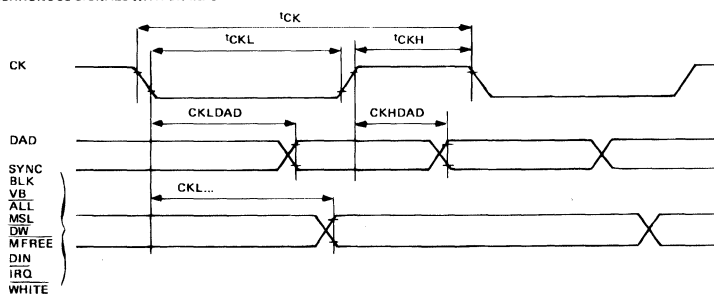
E88 EF9365-07

## MICROPROCESSOR BUS, READ ACCESS



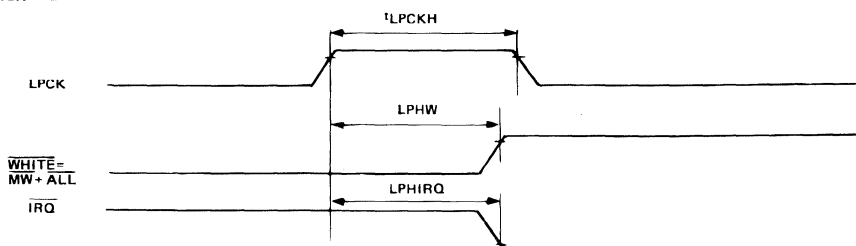
E88 EF9365-08

## SYNCHRONOUS SIGNALS WITH CK INPUT



E88 EF9365-09

## LIGHT PEN SIGNALS



E88 EF9367-04













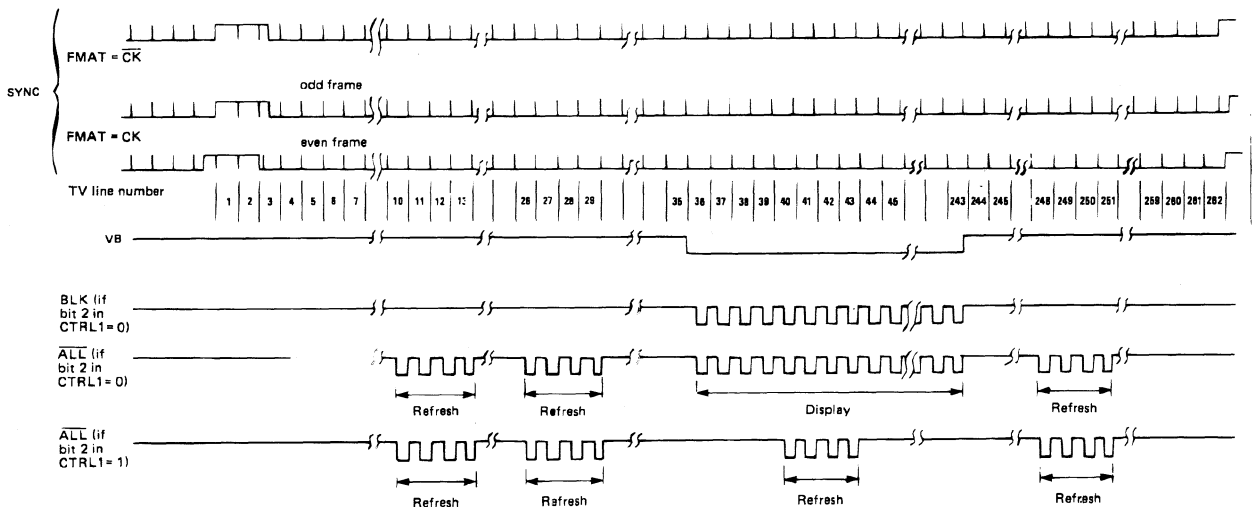








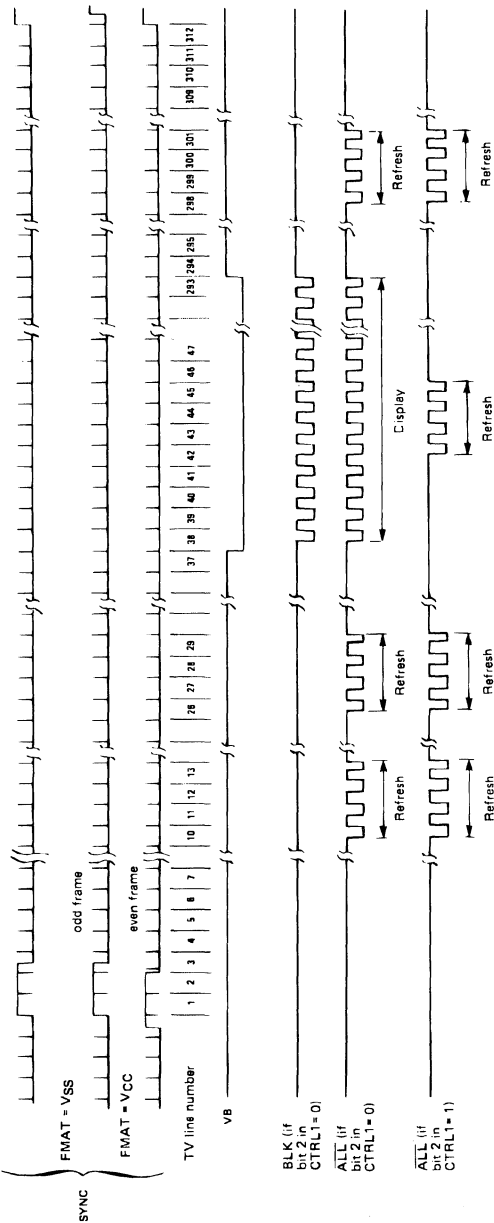
## FRAME SEQUENCE - 525 LINE SYNCHRONIZATION



Note:  $\overline{\text{ALL}}$  signal high denotes write periods.

E88 EF9367-09

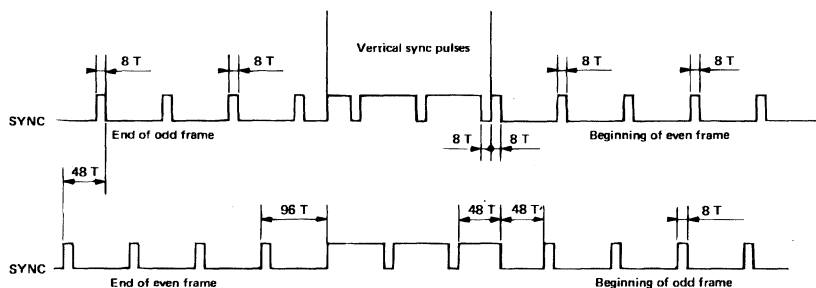
FRAME SEQUENCE - 625 LINE SYNCHRONIZATION



Note : ALL signal high denotes write periods.

## COMPOSITE SYNC AROUND FRAME SYNC

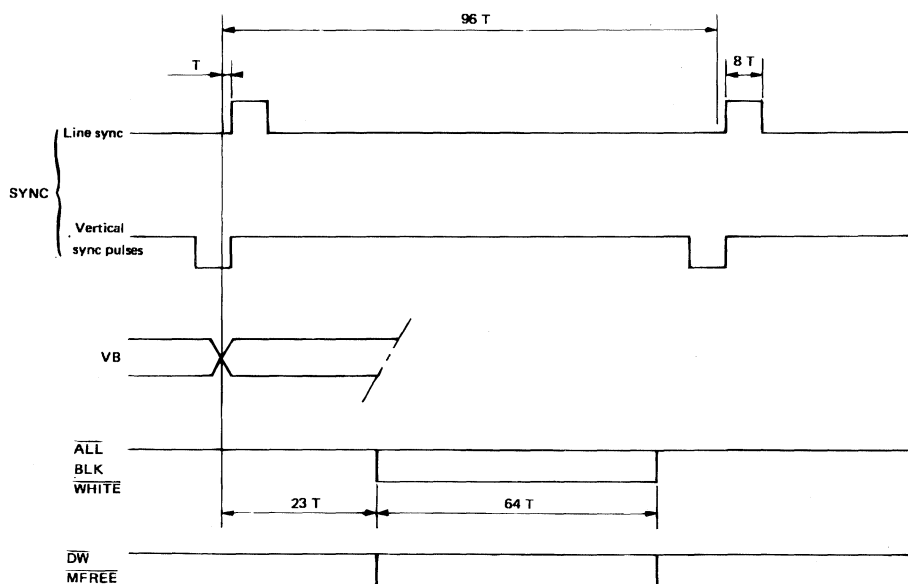
T : CK input period (667 ns in typical application where TV line duration is 64  $\mu$ s)



**Note :** If FMAT is low or tied to  $\overline{CK}$ , the pattern of the second line is repeated for each frame.

E88 EF9367-11

### DETAILED LINE DIAGRAM



E88 EF9367-12



























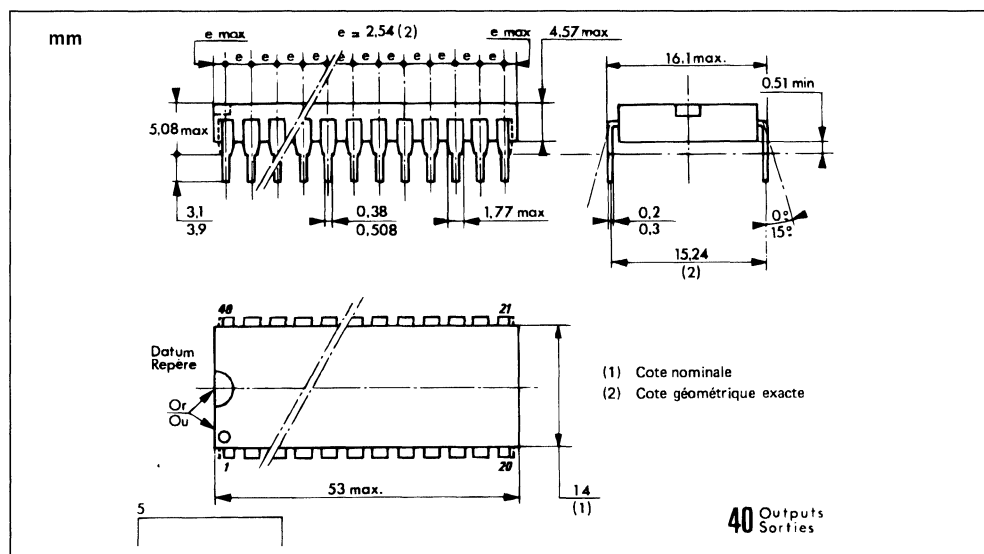






## PACKAGE MECHANICAL DATA

40 PINS - PLASTIC DIP









## TABLE OF CONTENTS

1. GENERAL OPERATION
2. COMMANDS
3. MICROPROCESSOR INTERFACE
4. THE VIDEO TIMING GENERATOR RAM REFRESH AND DISPLAY PROCESS
5. MEMORY ORGANIZATION
6. TIMING DIAGRAM
7. REGISTER MAP AND COMMAND TABLE
8. ORDERING INFORMATION AND PACKAGE MECHANICAL DATA

## **1. GENERAL OPERATION**

### **1.1. INTRODUCTION**

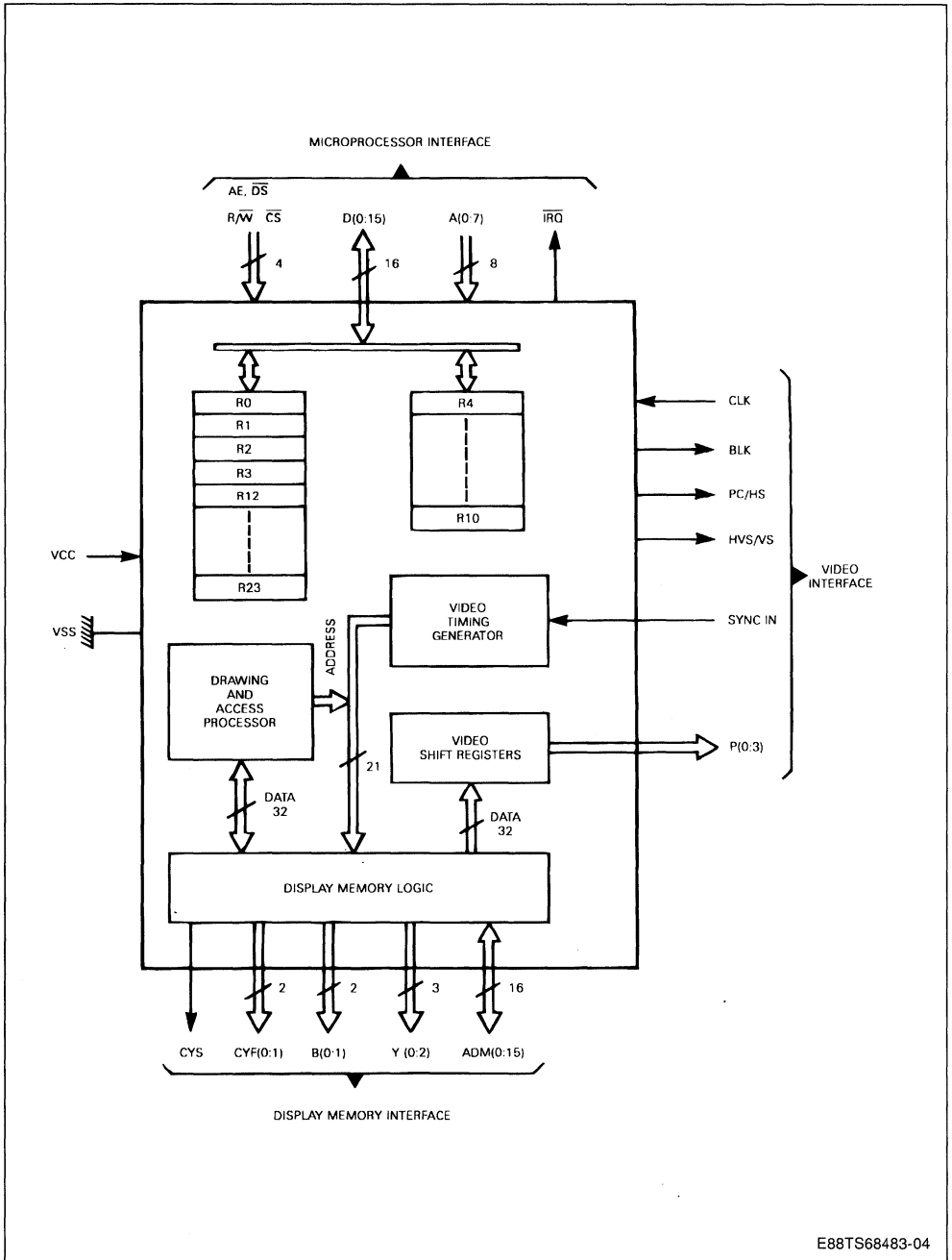
The TS68483 is an advanced color graphics controller chip. It is directly compatible with most popular 8 or 16-bit microprocessors.

Its display memory, containing the frame buffer and the character generators, may be assembled from standard dynamic RAM components.

On-chip video shift registers and fully programmable Video Timing Generator allow the TS68483 to be used in a wide range of terminals or computer design.

Additional informations on applications can be found in the TS68483 User's Manual.

## BLOCK DIAGRAM



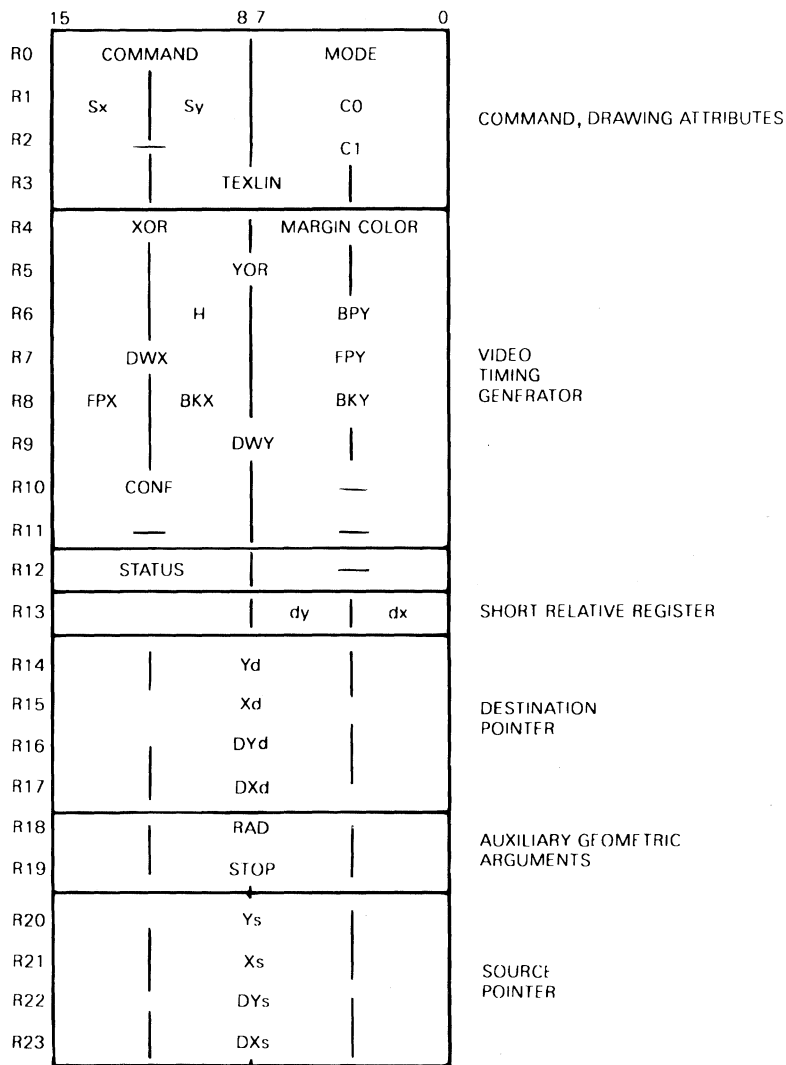
E88TS68483-04







Figure 1.2. : Register Map.



E88TS68483-05



Figure 1.3. : Cyclical Drawing Coordinates to Display Memory Mapping.

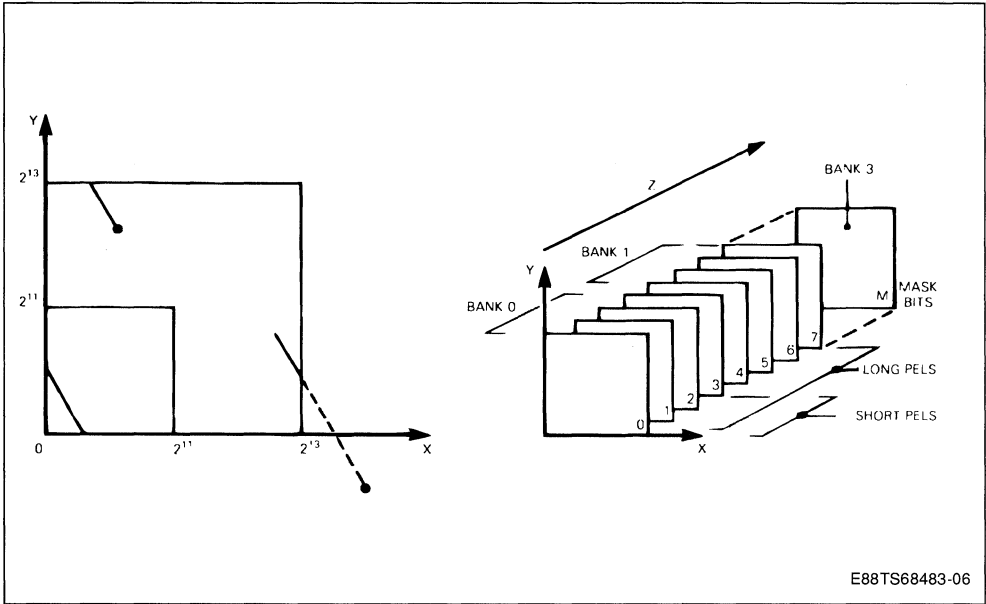


Figure 1.4. : The Display Memory Addressing Space.

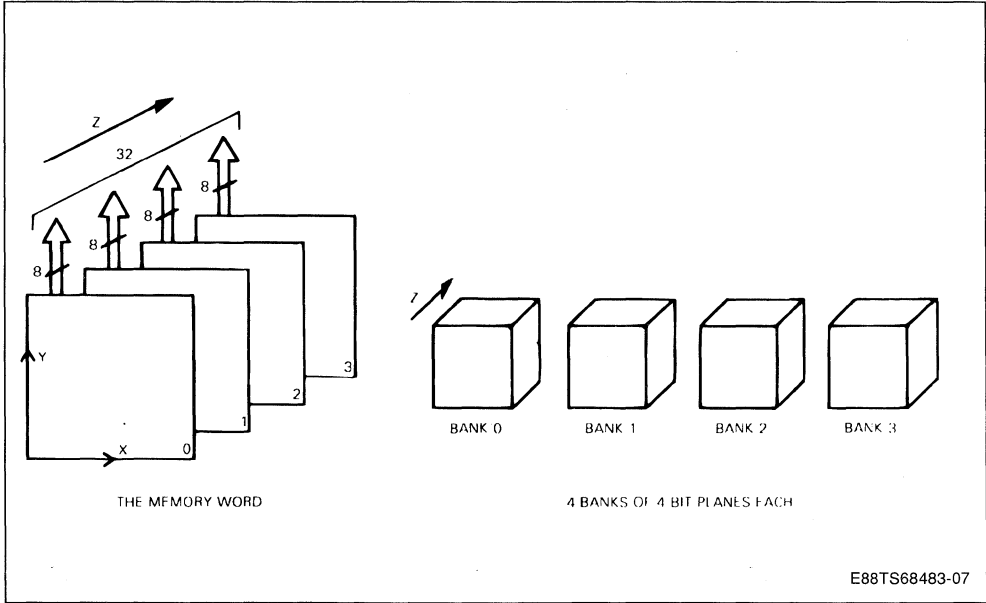
















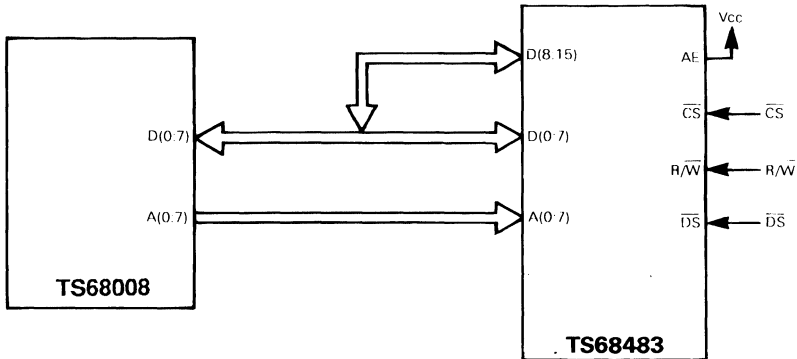






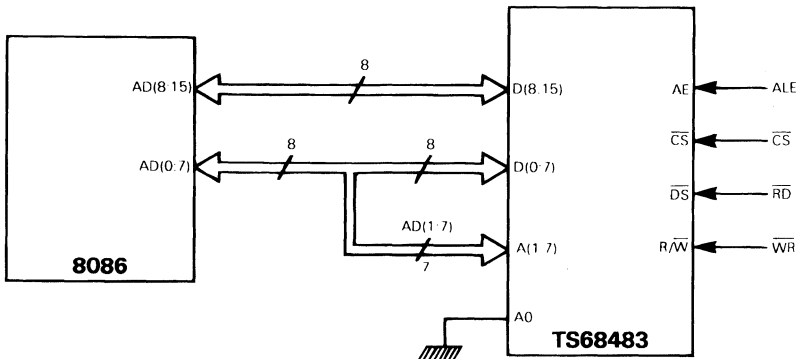


Figure 3.4. : Interface with TS68000/68008 MPU (continued).



E88TS68483-21

Figure 3.5. : Interface with 8086/8088 MPU.

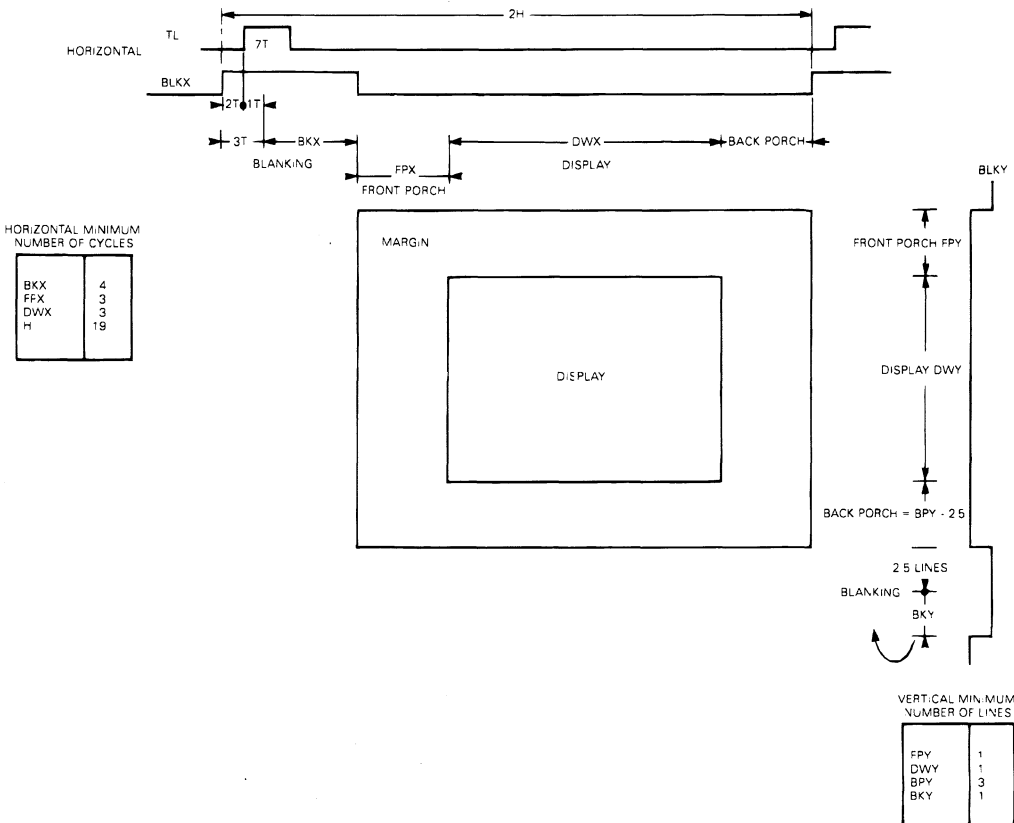


E88TS68483-22





Figure 4.1 : Video Programming.



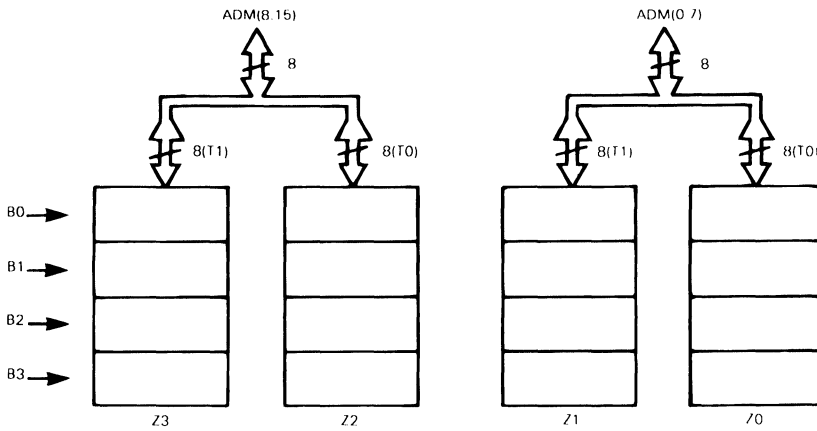
E881TS68483-24





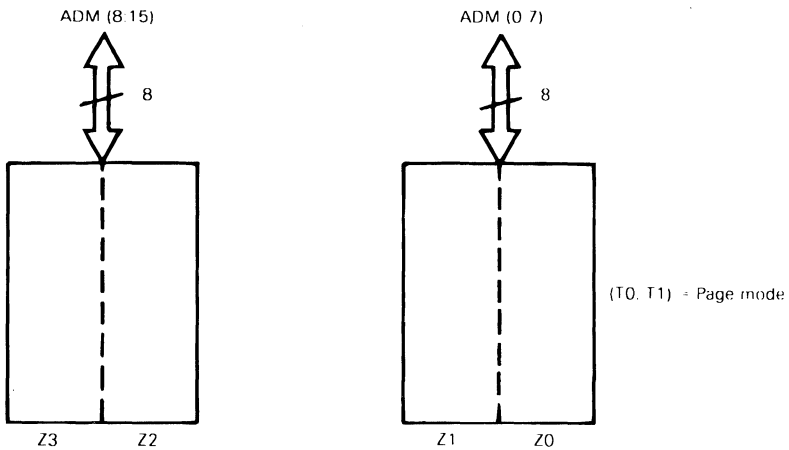


## ONE BLOCK-ONE Z



E88TS68483-25

## ONE BLOCK-TWO Z



E88TS68483-26



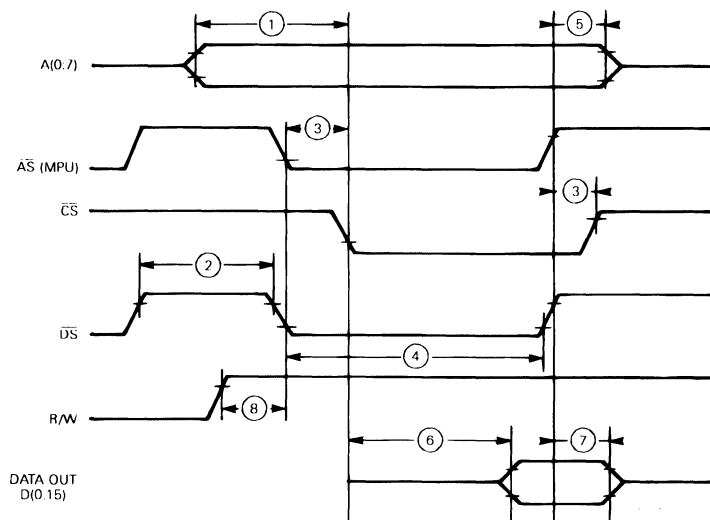






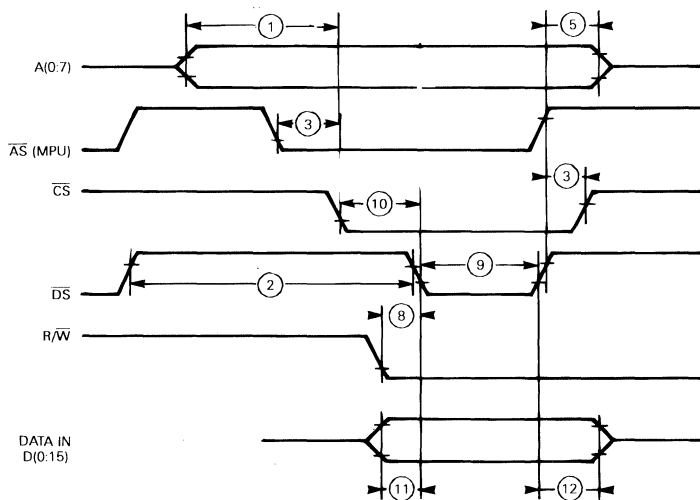
## UNMUX MODE

## READ CYCLE



E88TS68483-30

## WRITE CYCLE

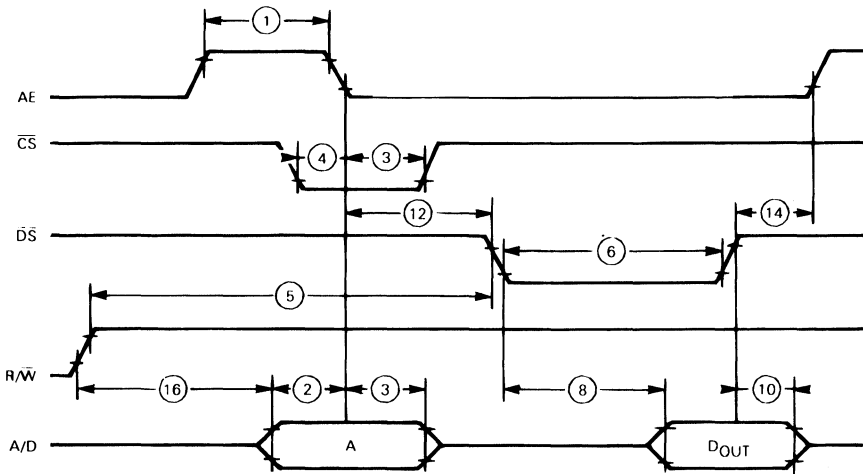


E88TS68483-31



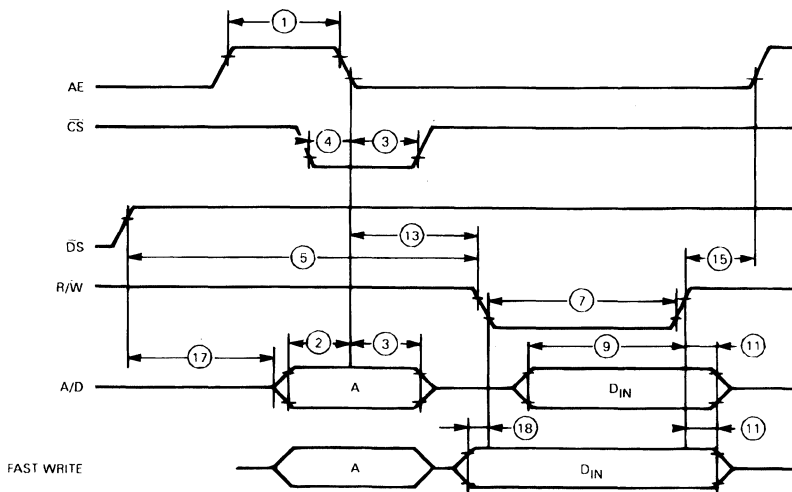
## MUX MODE

## READ CYCLE



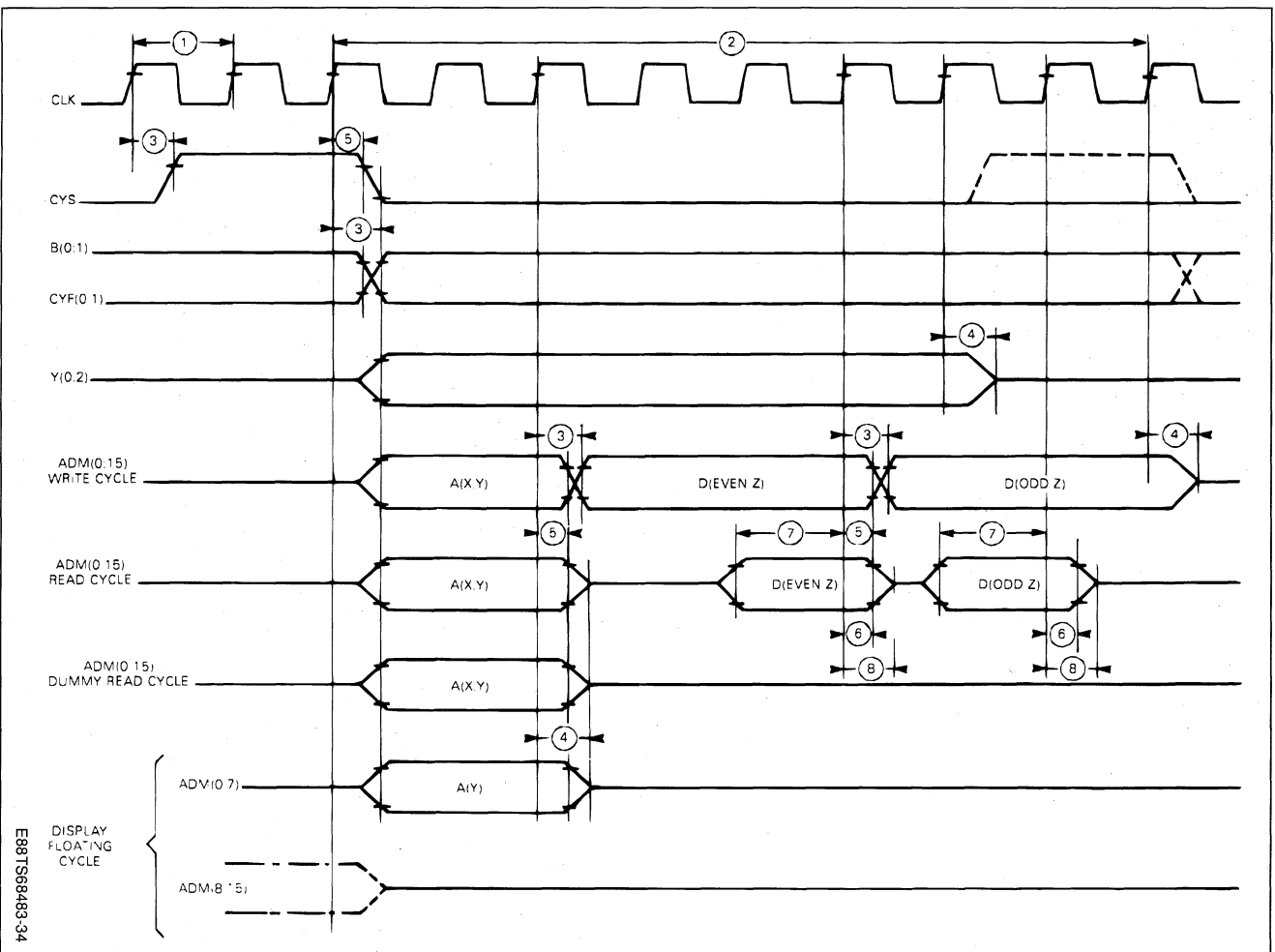
E88TS68483-32

## WRITE CYCLE



E88TS68483-33

## MEMORY INTERFACE



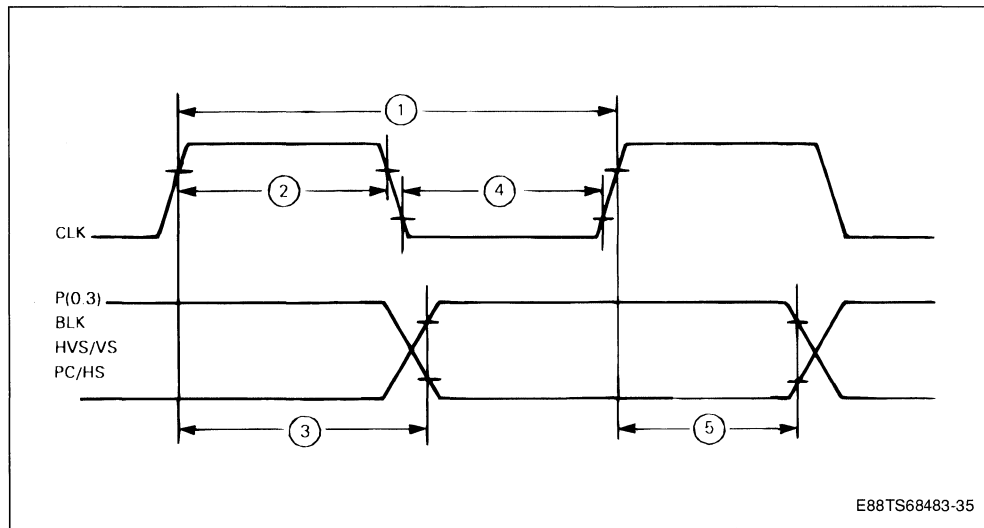
E88TS68483-34

## 6.3. VIDEO INTERFACE

P0, P1, P2, P3, BLK, HVS/VS, PC/HS

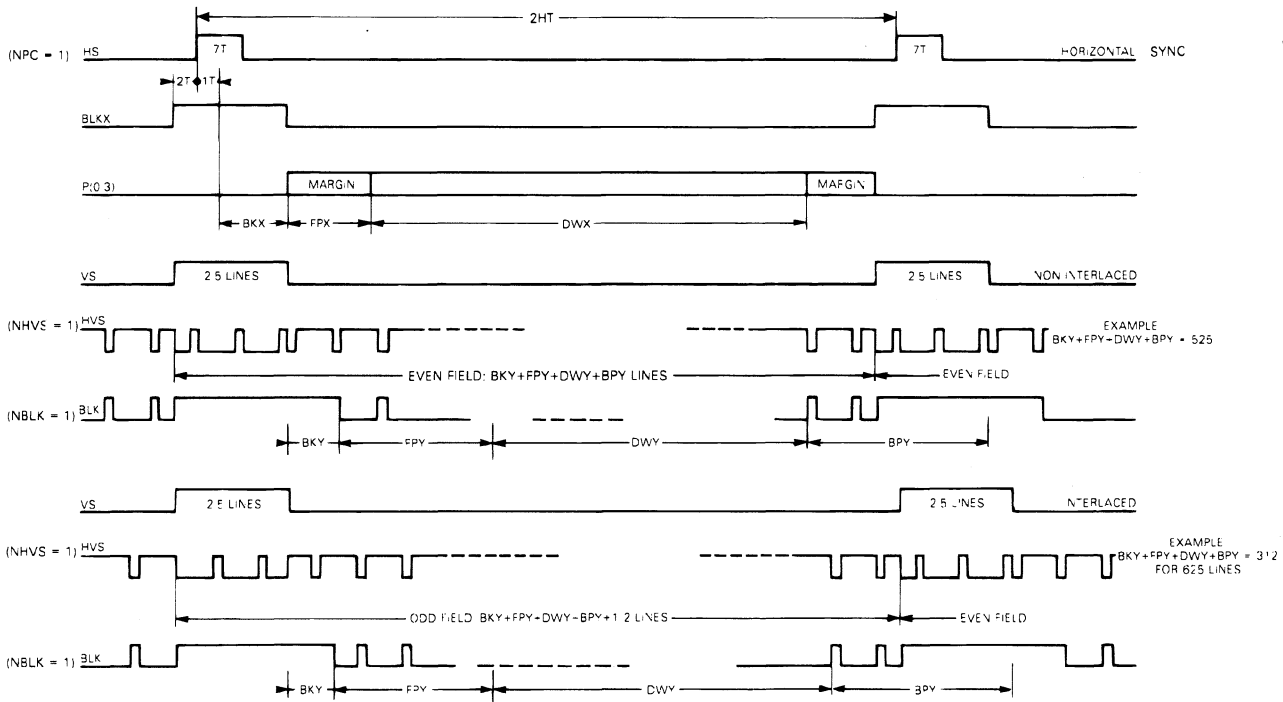
 $V_{CC} = 5.0\text{ V} \pm 5\%$ ,  $T_A = T_L$  to  $T_H$ , CLK duty cycle = 50 %Reference levels :  $V_{IL} = 0.8\text{ V}$  and  $V_{IH} = 2\text{ V}$ ,  $V_{OL} = 0.4\text{ V}$  and  $V_{OH} = 2.4\text{ V}$ ,  $C_L = 50\text{ pF}$ 

TIMING DIAGRAM 4.



Indent Number	Parameter	TS68483-15		TS68483-18		Unit
		Min.	Max.	Min.	Max.	
1	TCLK : CLK Period	66	166	55	166	ns
2	CLK High Pulse Width	28		23		ns
3	Output Delay from CLK Rising Edge		40		30	ns
4	CLK Low Pulse Width	28		23		ns
5	Output Hold Time	10		10		ns

## SYNCHRONISATION SIGNAL OUTPUTS



E88TS68483-36



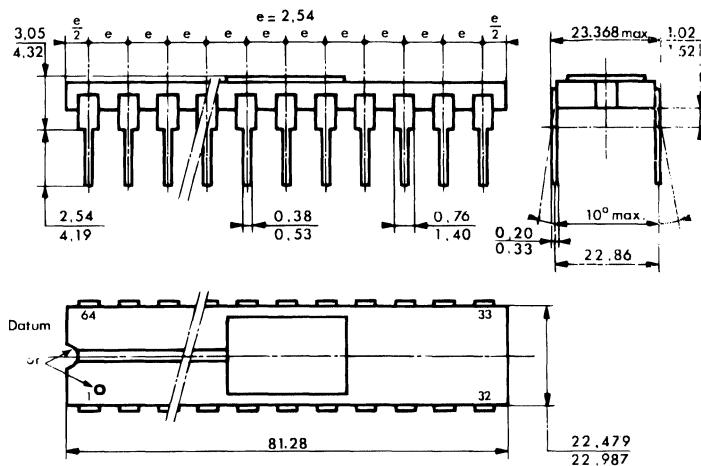








## 64 PINS – PLASTIC DIP





# **COLOR PALETTE**











**TIMING DIAGRAM 1 - MULTIPLEXED MODE - MOTOROLA TYPE (SMI = V<sub>SS</sub>)**

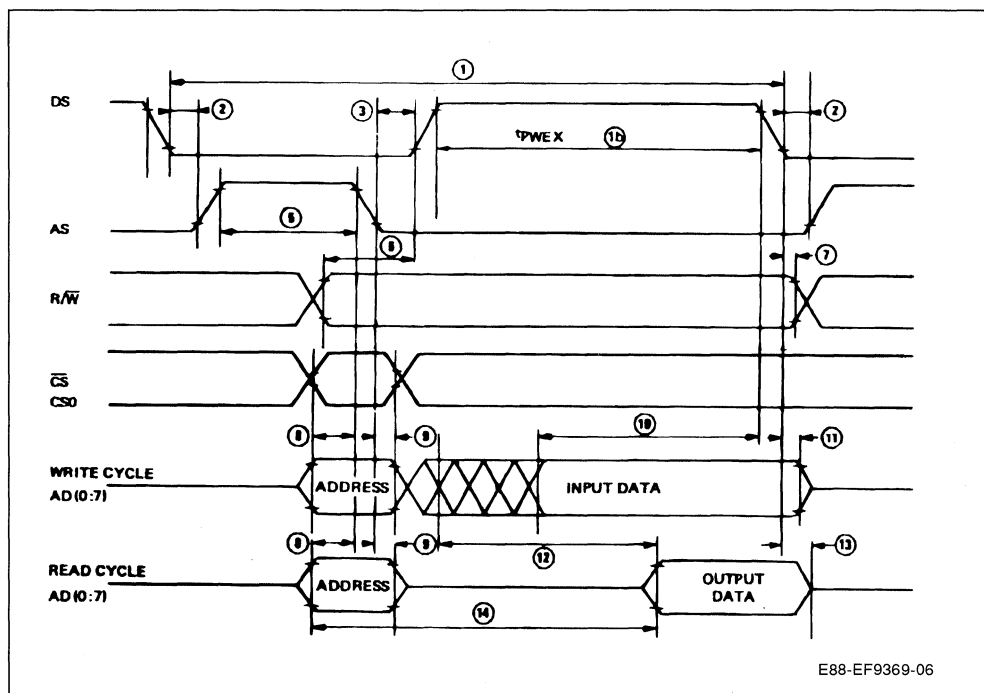










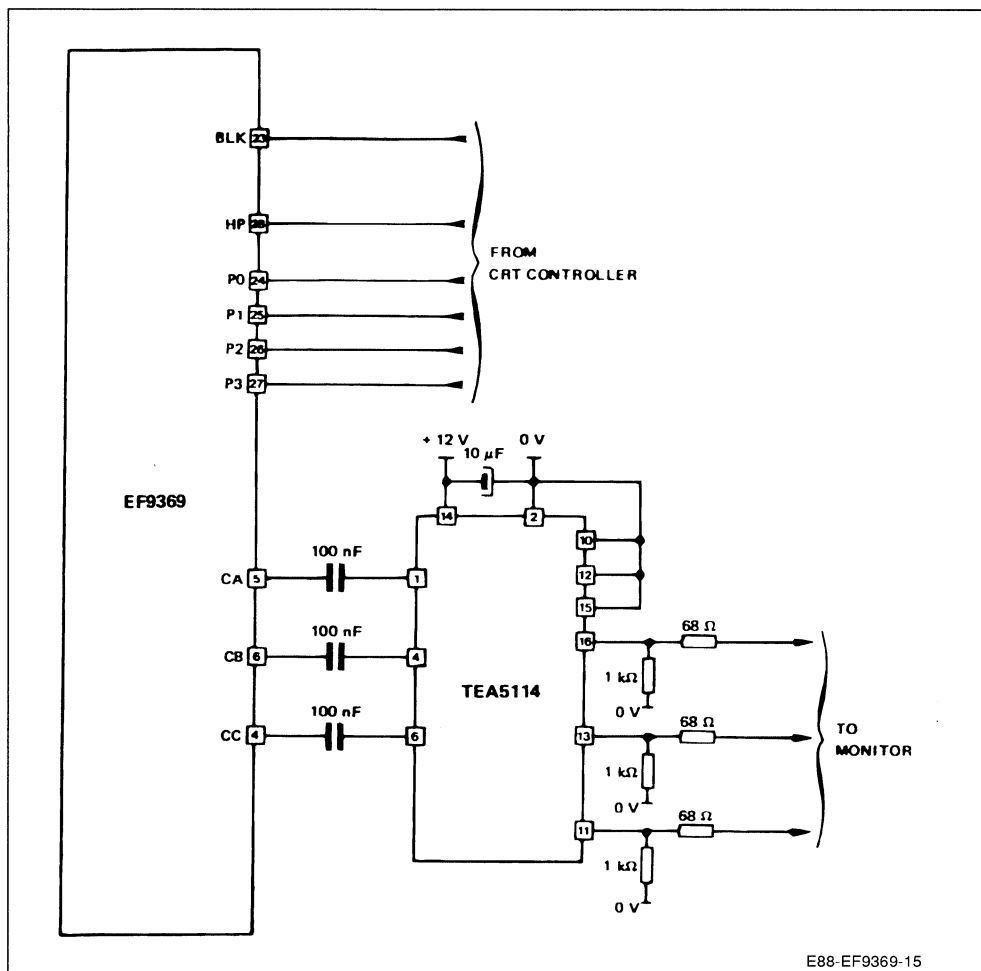










Figure 2 : Typical 1 V - 75  $\Omega$  Video Interface

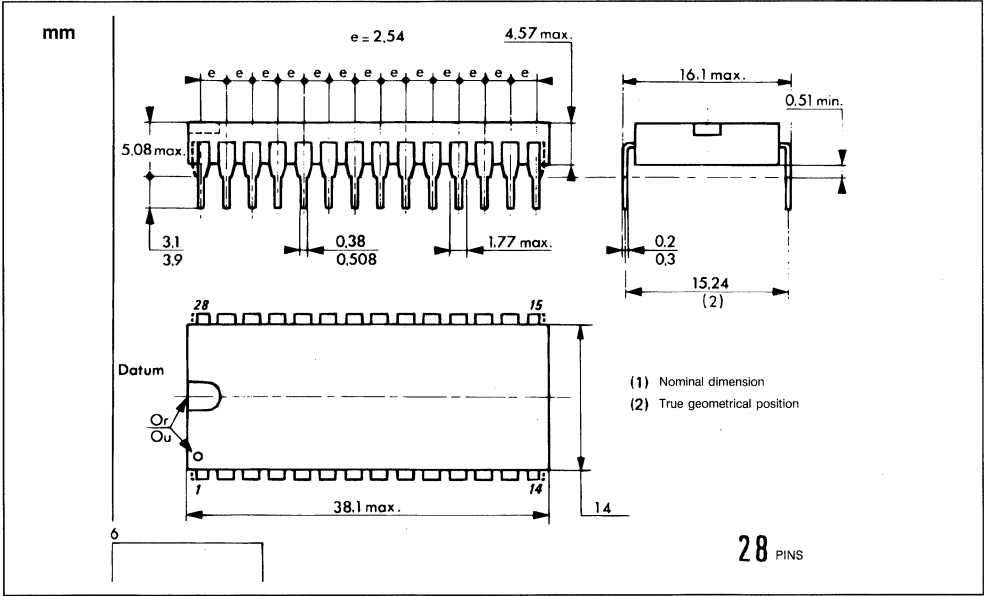
**Note :** Each digital or analog ground must be separately connected to EF9369 pin 1.

ORDERING INFORMATION

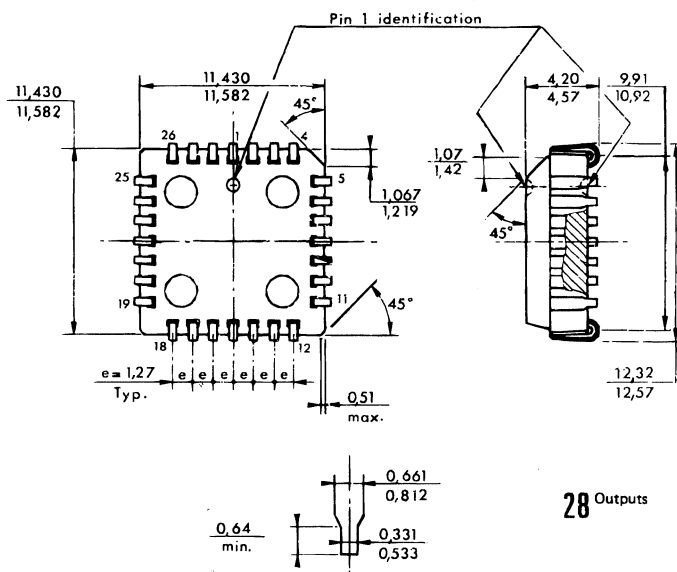
Part Number	Temperature	Package
EF9369P	0 to 70 °C	DIP28
EF9369P30	0 to 70 °C	DIP28
EF9369FN	0 to 70 °C	PLCC28

PACKAGE MECHANICAL DATA

28 PINS - PLASTIC DIP



## 28 PINS - PLASTIC LEADED CHIP CARRIER

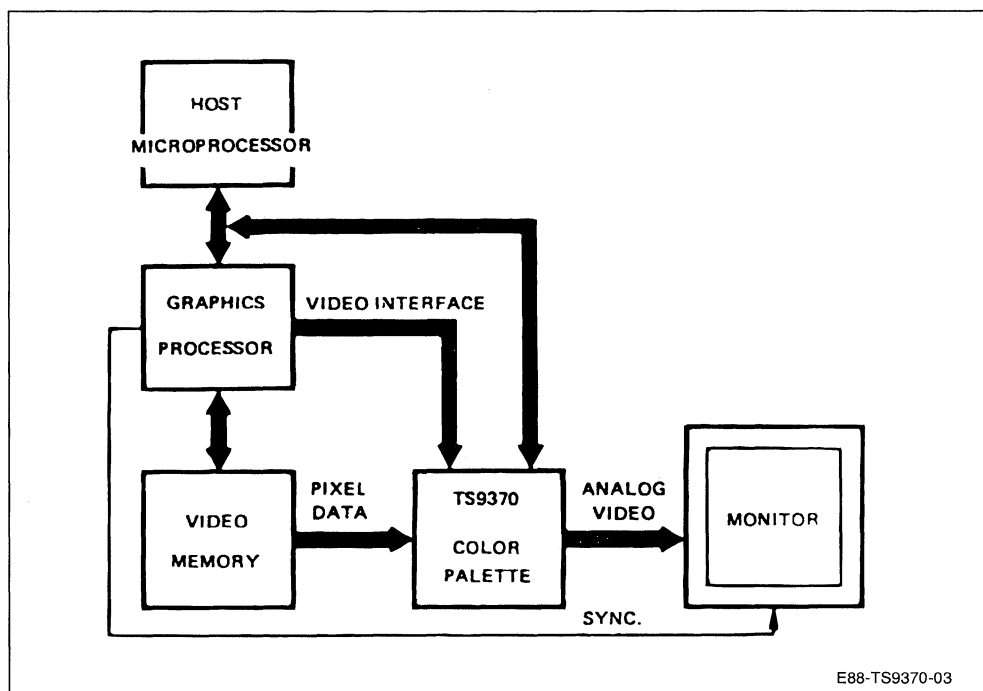




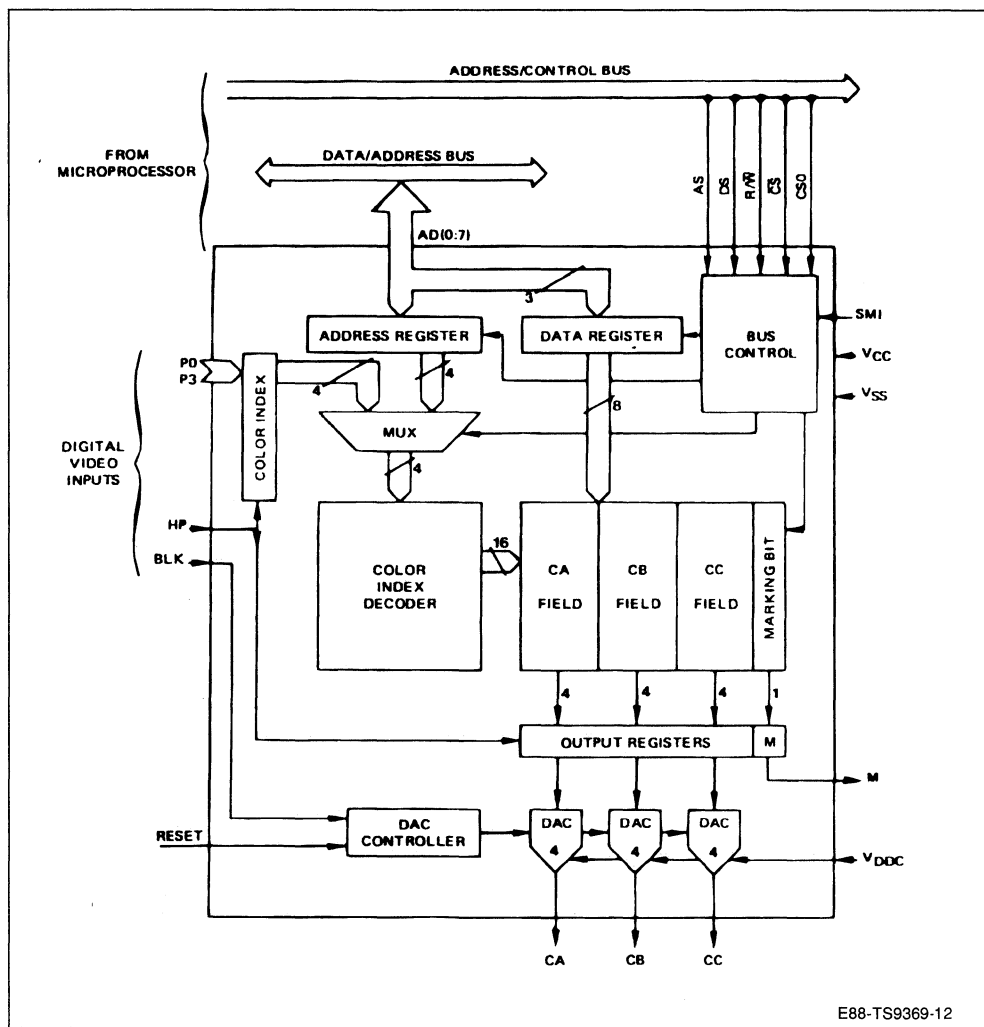




## TYPICAL APPLICATION



## BLOCK DIAGRAM

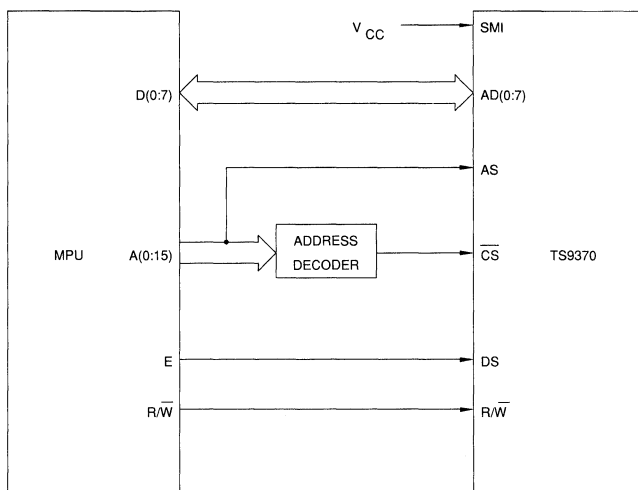




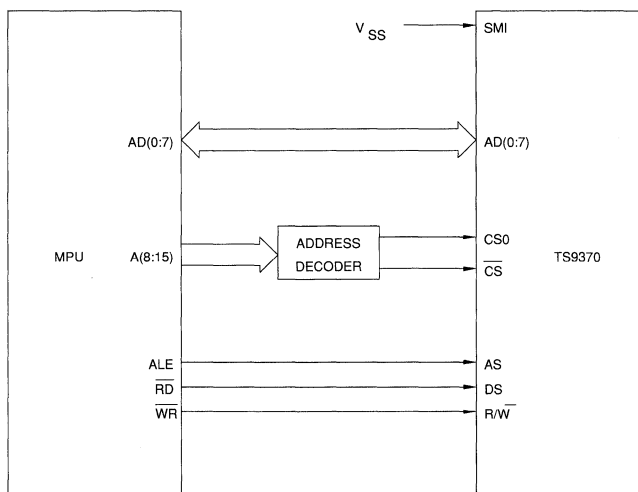




## NON MULTIPLEXED MODE



## MULTIPLEXED MODE - INTEL TYPE



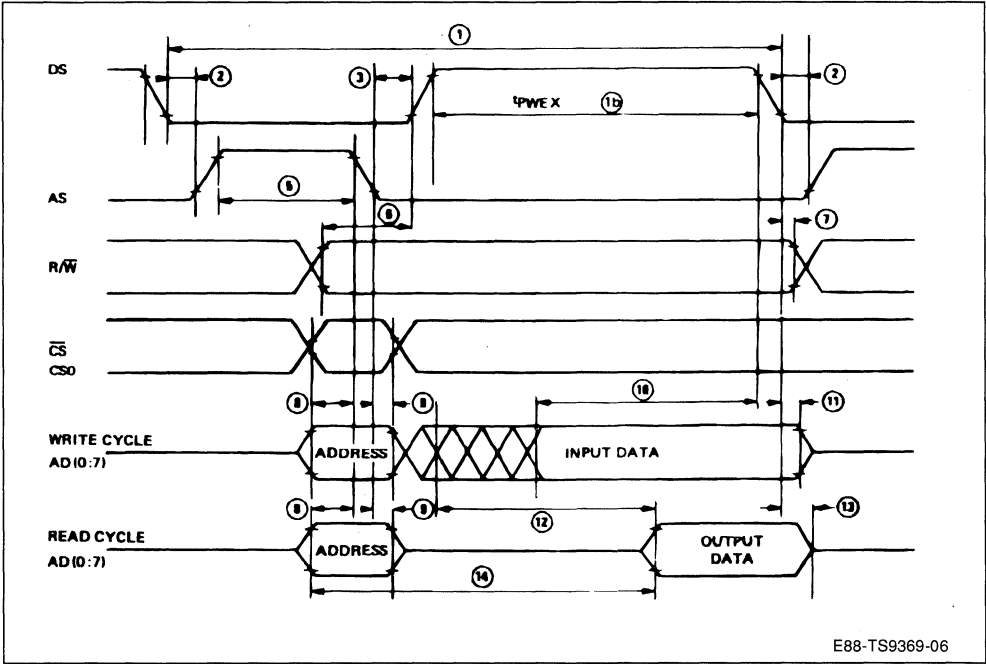
E88-EF9369-12







TIMING DIAGRAM 1 - MULTIPLEXED MODE - MOTOROLA TYPE (SMI = V<sub>SS</sub>)









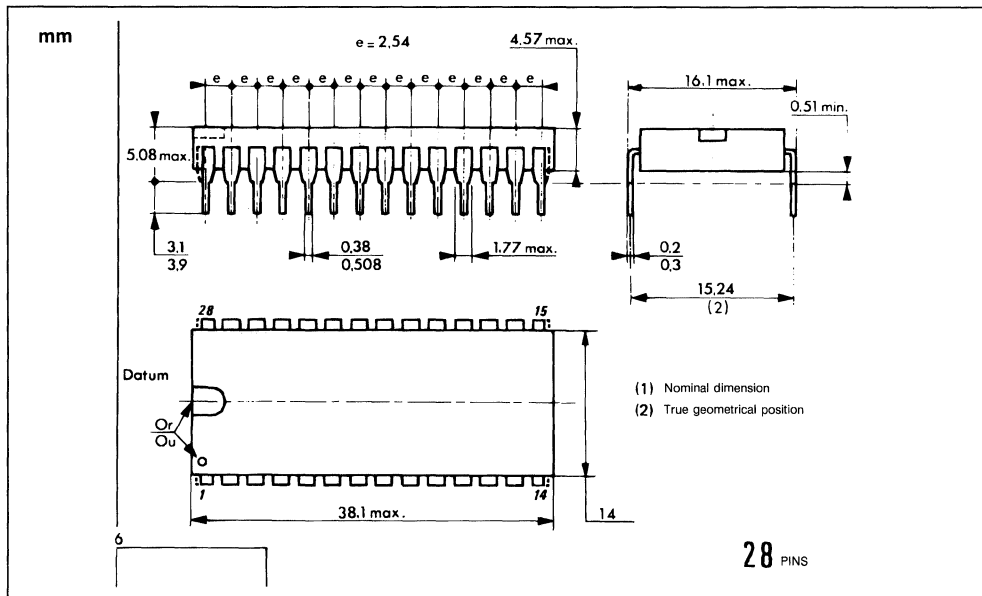


## ORDER INFORMATION

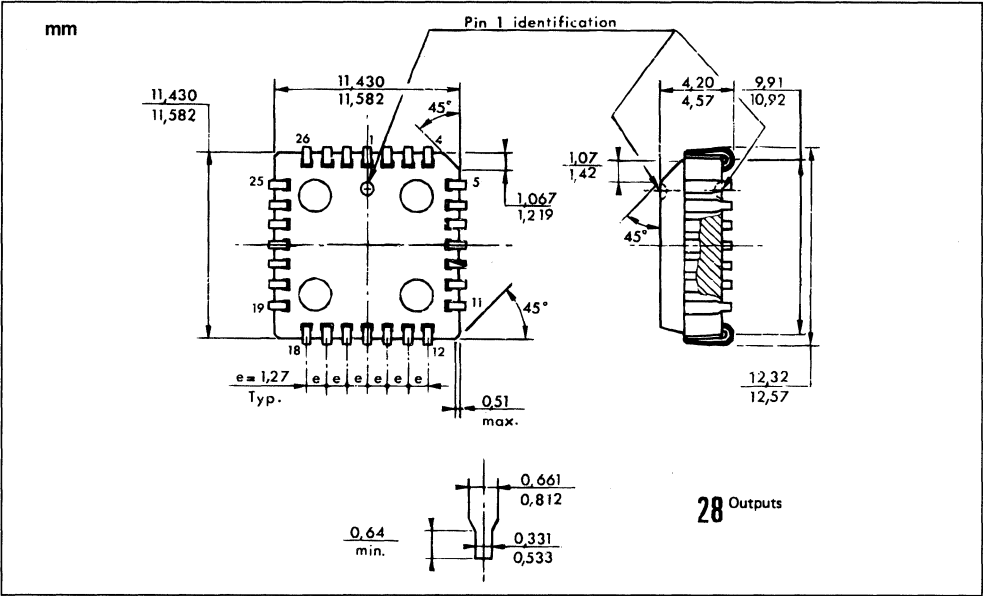
Part Number	Temperature	Package
TS9370IP20	- 25 °C to + 85 °C	DIP28
TS9370IFN20	- 25 °C to + 85 °C	PLCC28
TS9370IP30	- 25 °C to + 85 °C	DIP28
TS9370IFN30	- 25 °C to + 85 °C	PLCC28
TS9370CP45	0 °C to 70 °C	DIP28

## PACKAGE MECHANICAL DATA

28 PINS - PLASTIC DIP



28 PINS - PLASTIC LEADED CHIP CARRIER



## **APPLICATION NOTES**



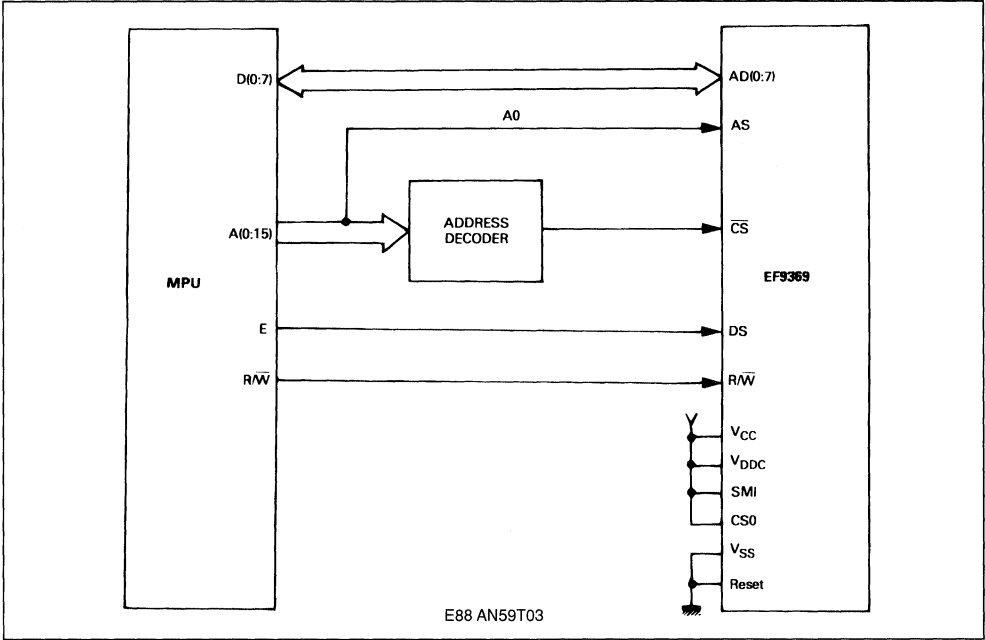








Figure 3.1: Non-multiplexed Mode - Motorola Type Microprocessor.



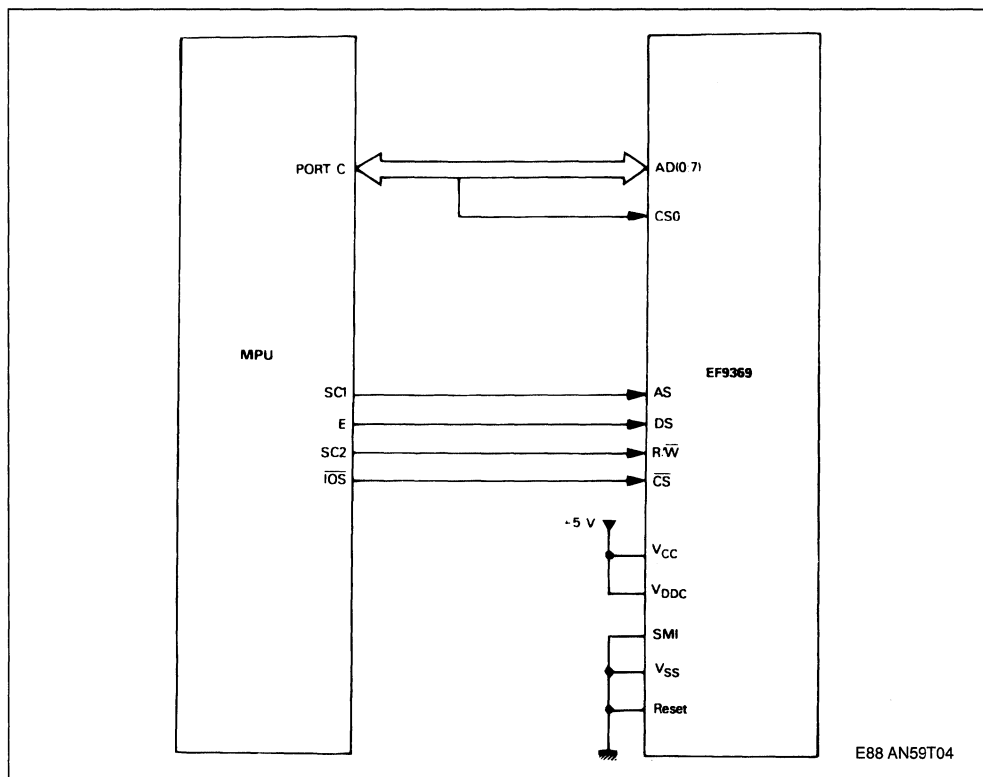
**Figure 3.2 : Multiplexed Mode - Motorola Type Microprocessor.**



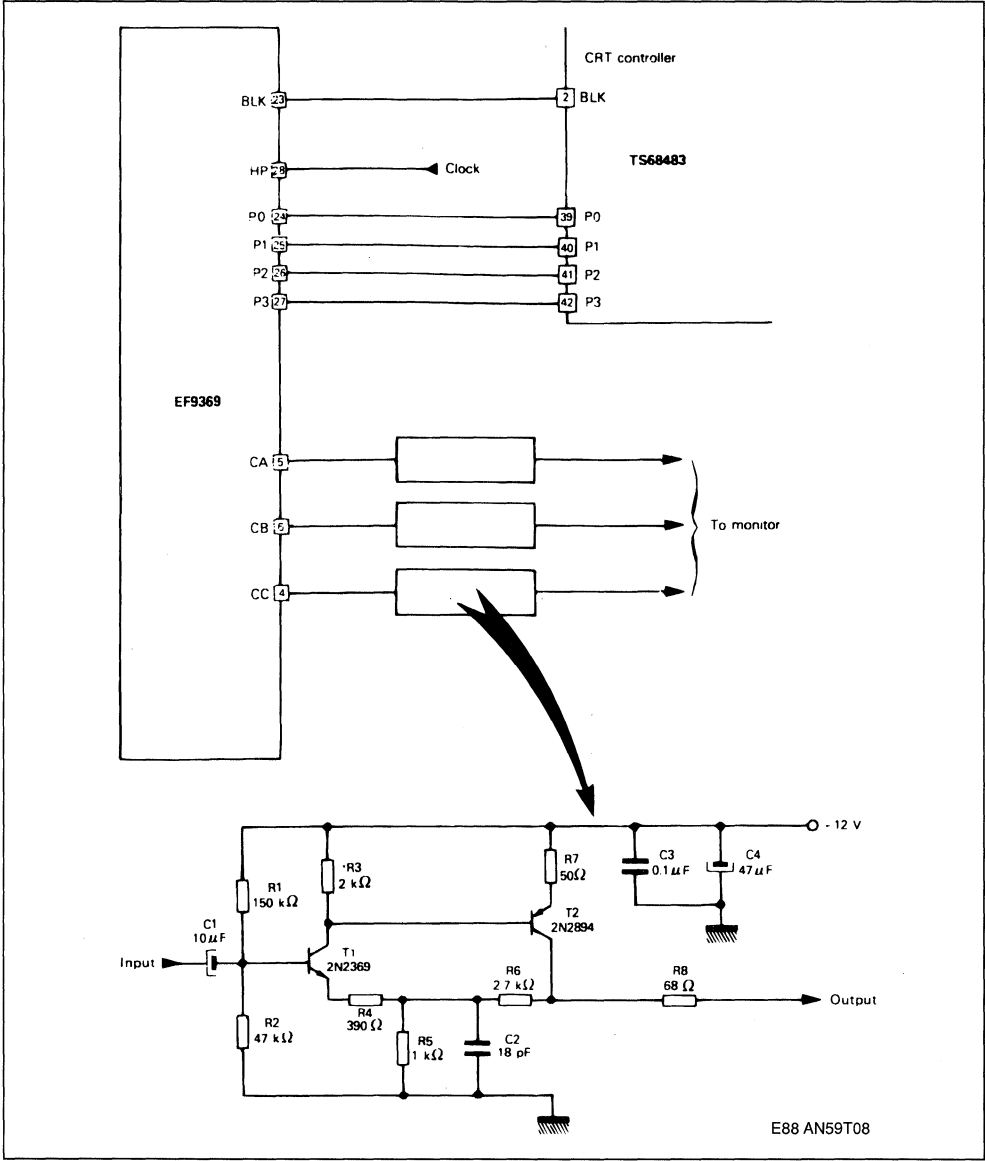








Figure 5.2.





With the EF9369 each "primary color" can get sixteen different values which give the possibility of choosing a tint amongst 4096.

### A FEW EXAMPLES

The sixteen values will go from 0 to F for each "primary color" in the CLUT.

- Dark and light :

Cyan is the addition of green and blue. For a dark cyan each value of green and blue must be low.

Ex : green = 3, blue = 3, red = 0

For a light cyan the blue and green values must be high.

Ex : green = D, blue = D, red = 0

- Purple :

Ex : green = 6, blue = 9, red = 8

- Pink : high value of red and equal value of green and blue.

Ex : green = 3, blue = 3, red = D

- Orange :

Ex : green = 3, blue = 0, red = D

- Brown :

Ex : green = 3, blue = 1, red = F

All these examples are only indications. If other colors are needed, each value of each "primary color" must be changed in order to get the right one.

4096 possibilities are available !





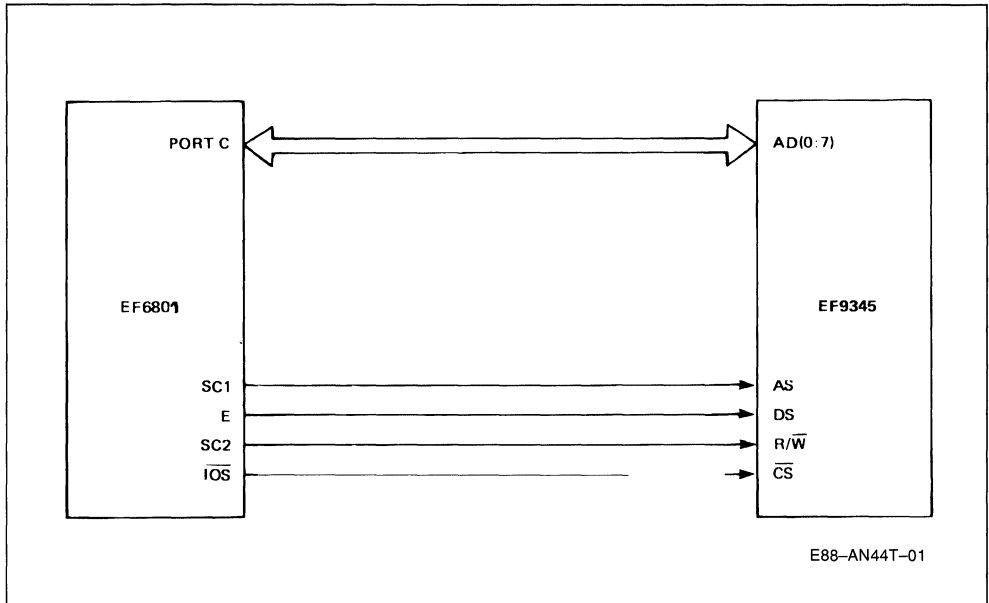
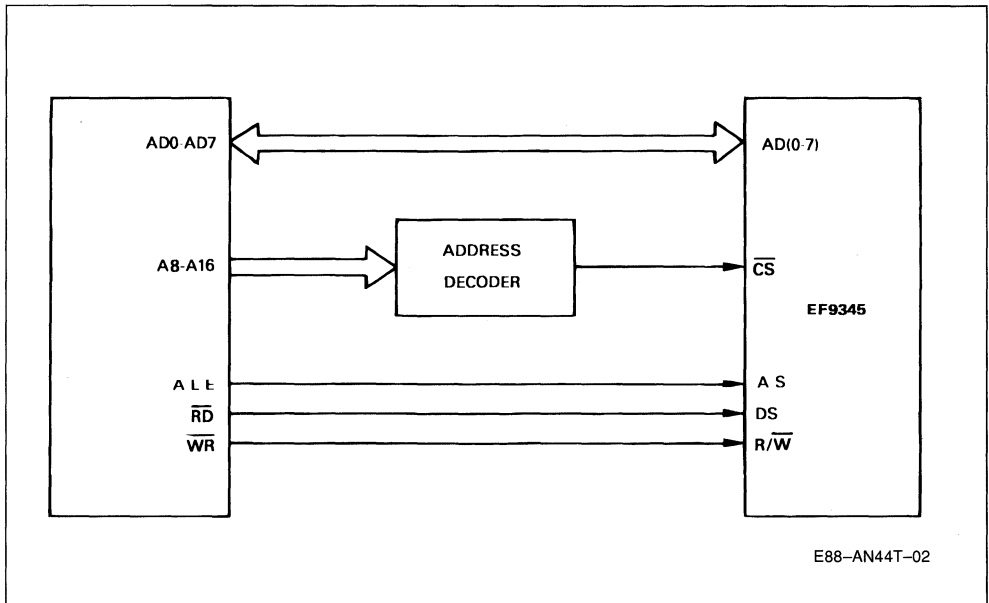
**Figure 1 :** Interface with EF6801.**Figure 2 :** Interface with a Multiplexed Bus Intel Type Microprocessor.





Figure 4 : Timing Diagram Associated with Figure 3.

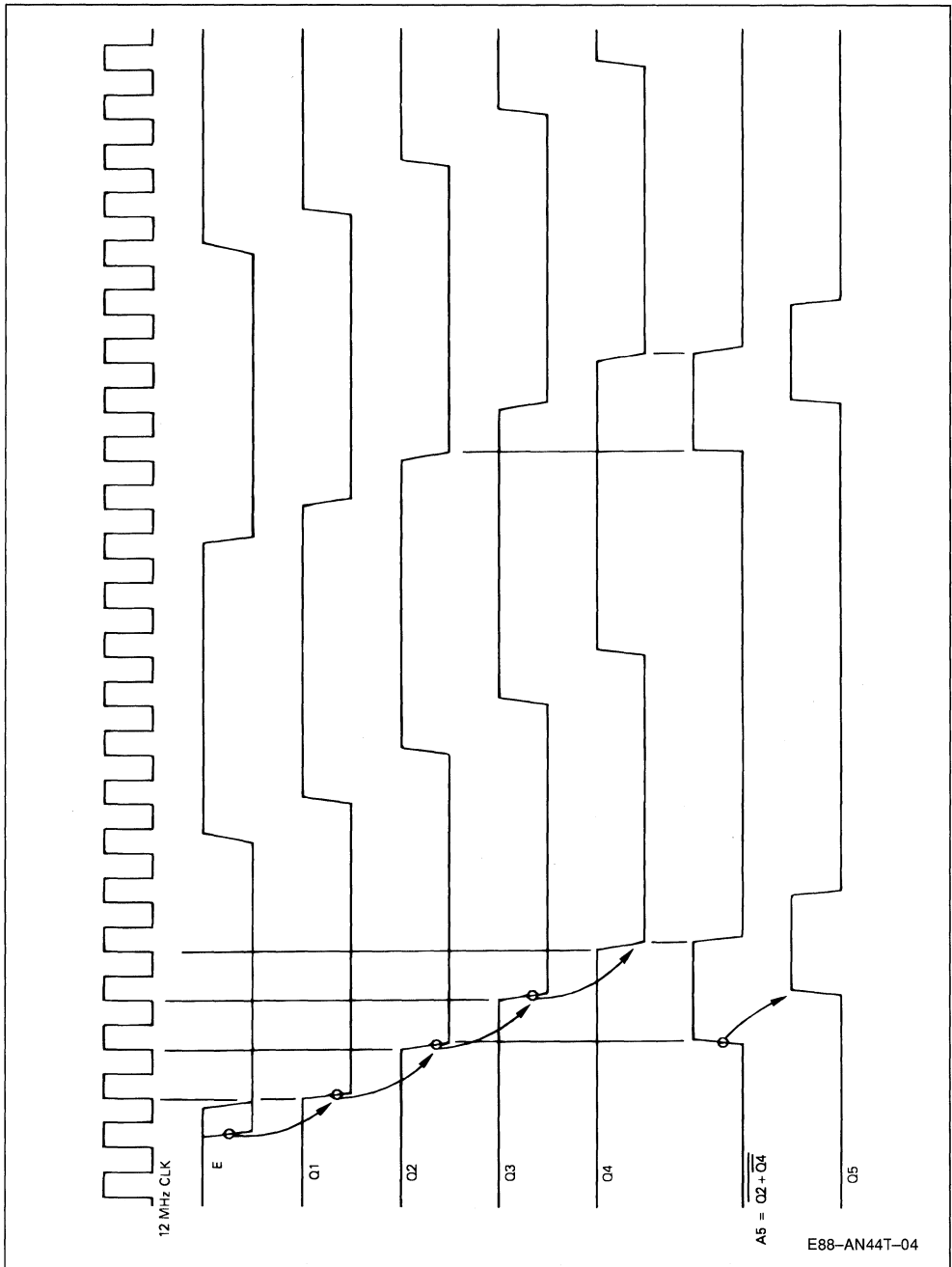


Figure 5 : Interface with EF6800/6809 without Multiplexing Address and Data Bus.

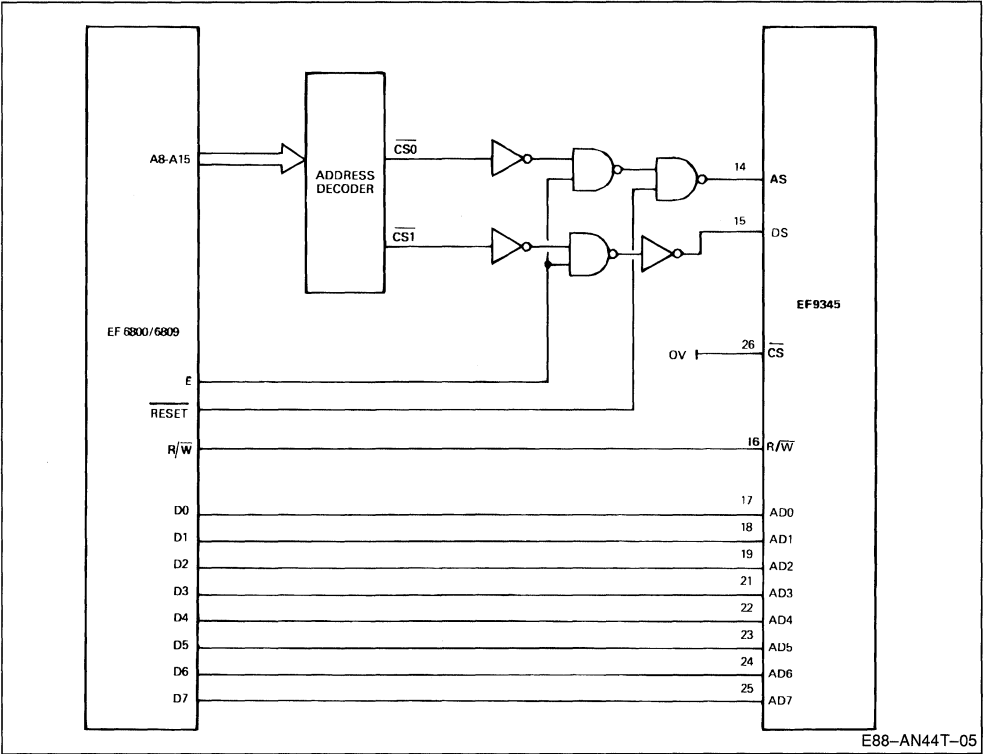


Figure 6 : Access to an EF9345 Register when Using the Non-Multiplexing scheme Interface.

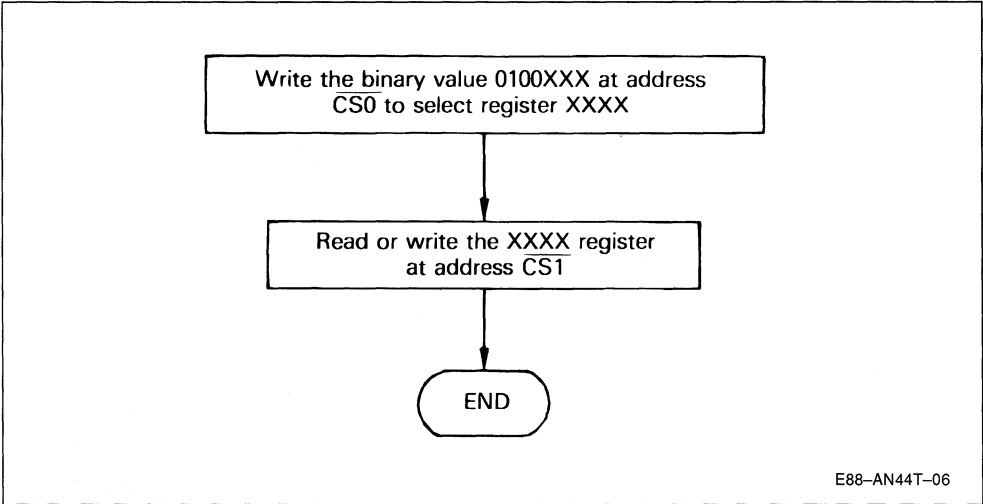
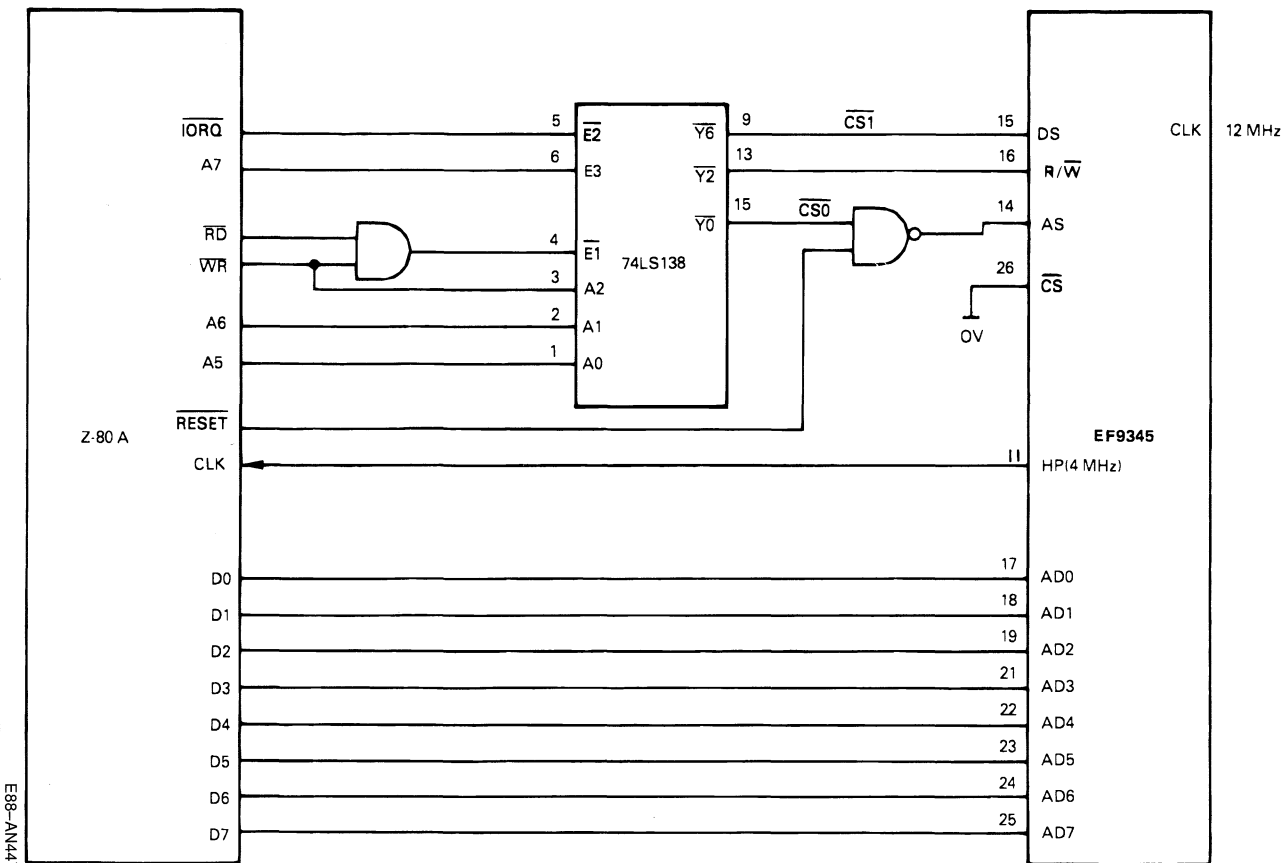


Figure 7 : EF9345 Interface with a Z-80 without Multiplexing Address and Data Bus.



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Figure 10 : Direct Access Registers.

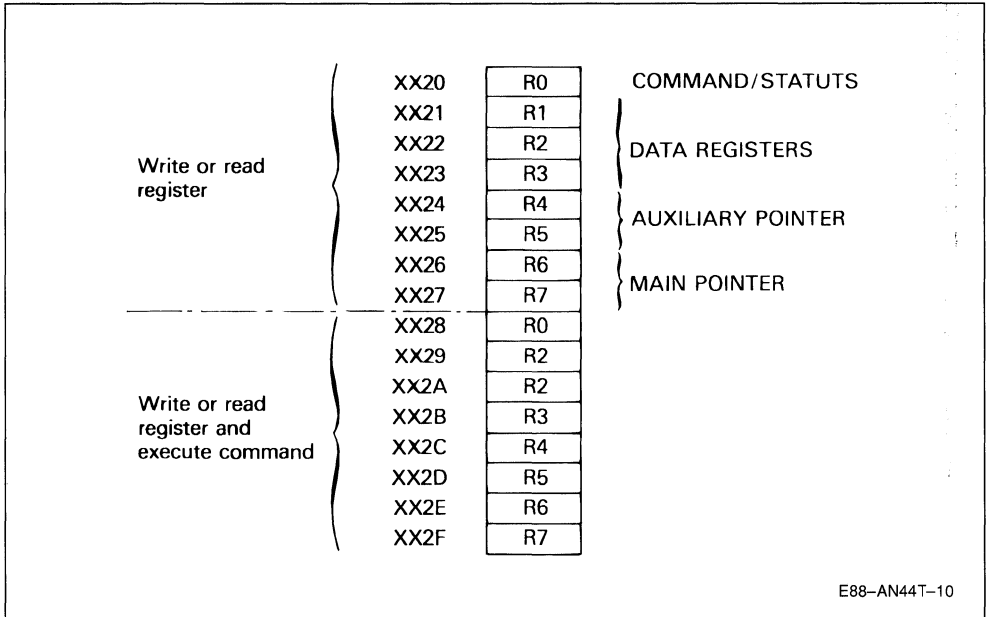


Figure 11 : Indirect Access Registers.

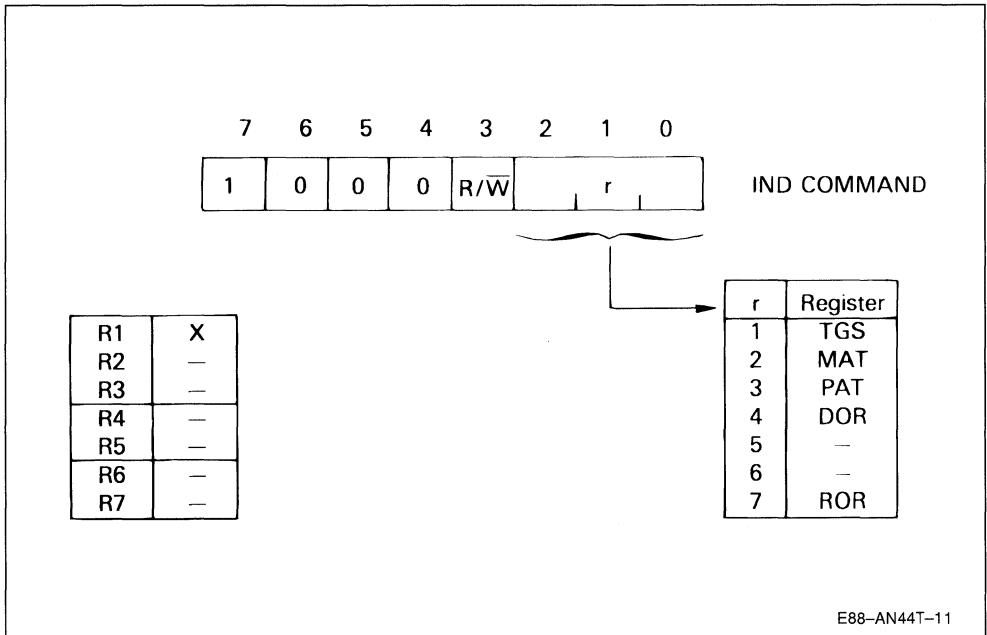
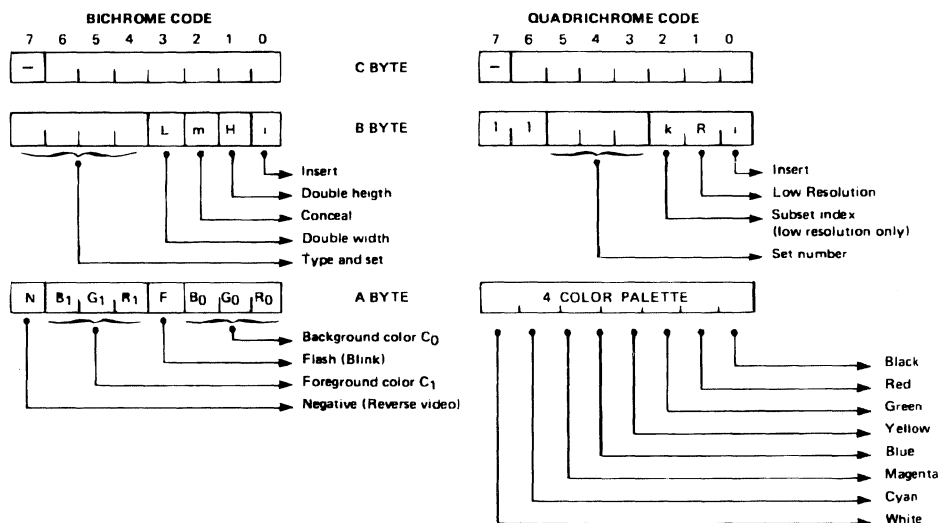






Figure 13 : 40 Char/Row Fixed Long Codes.



B	G	R	Color Value
0	0	0	Black
0	0	1	Red
0	1	0	Green
0	1	1	Yellow
1	0	0	Blue
1	0	1	Magenta
1	1	0	Cyan
1	1	1	White

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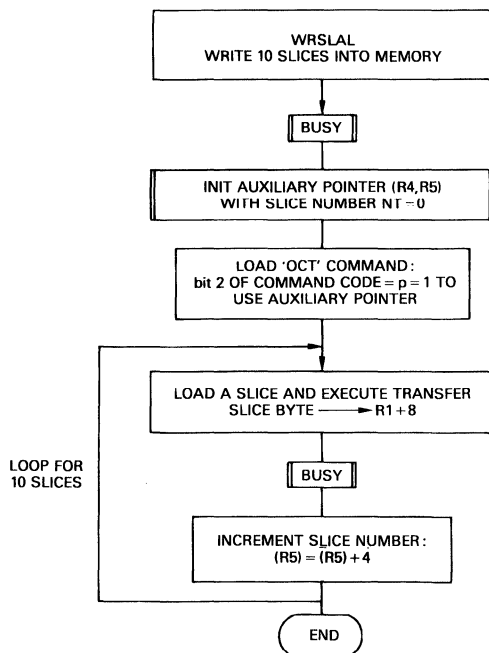








Figure 19 : UDS Slice Loading Flowchart.



NOTE: BIT Z3 OF BLOCK NUMBER MUST BE INITIALIZED IN R6(6).

**Note :** Bit Z3 of block number must be initialized in R6(6).

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Figure 20 : 80 Char/Row Character Code.

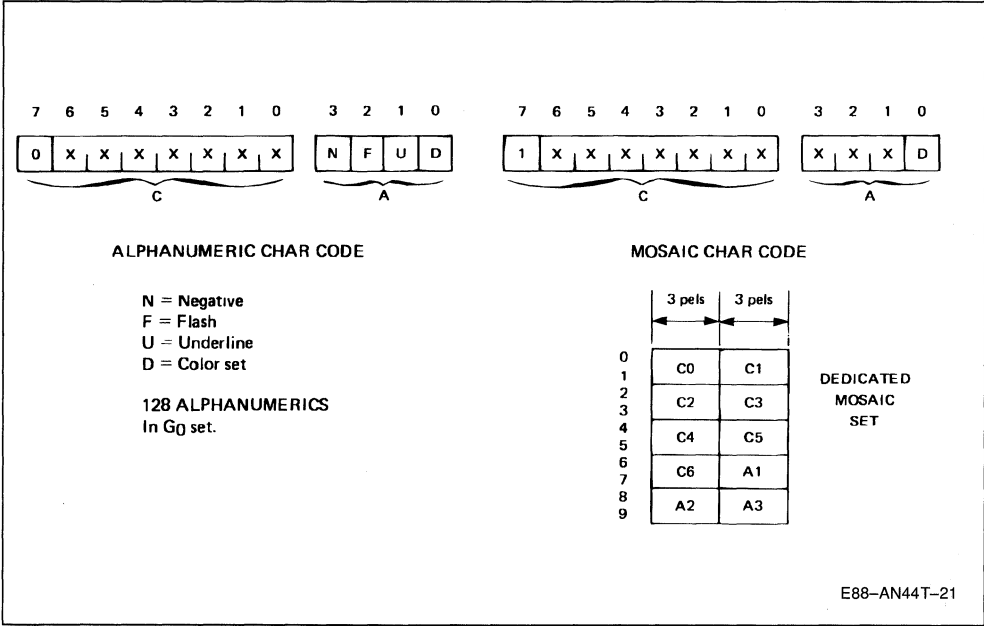
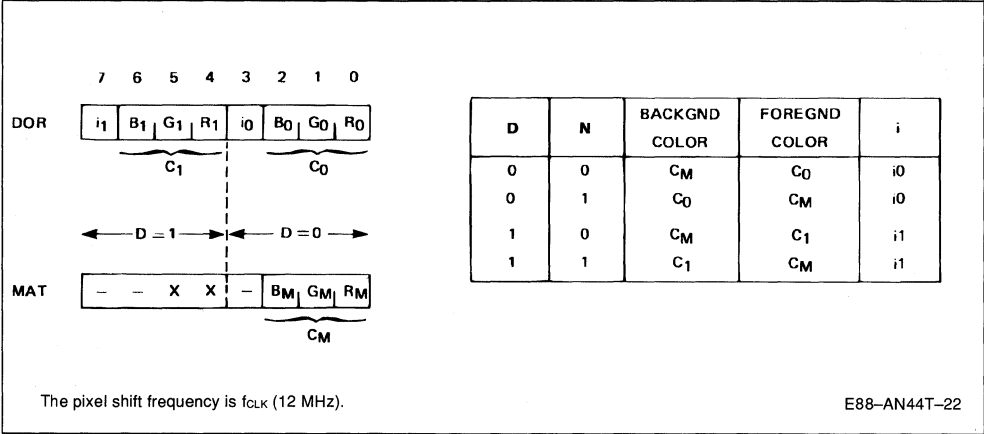
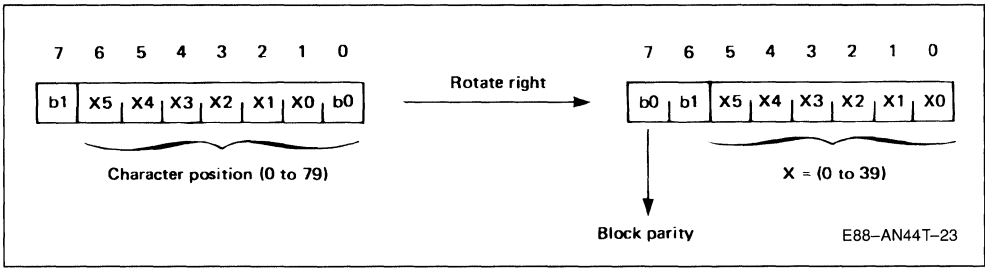


Figure 21 : Color Selection.



**Figure 22** : Transcoding an Horizontal Screen Location into a R7 Pointer.











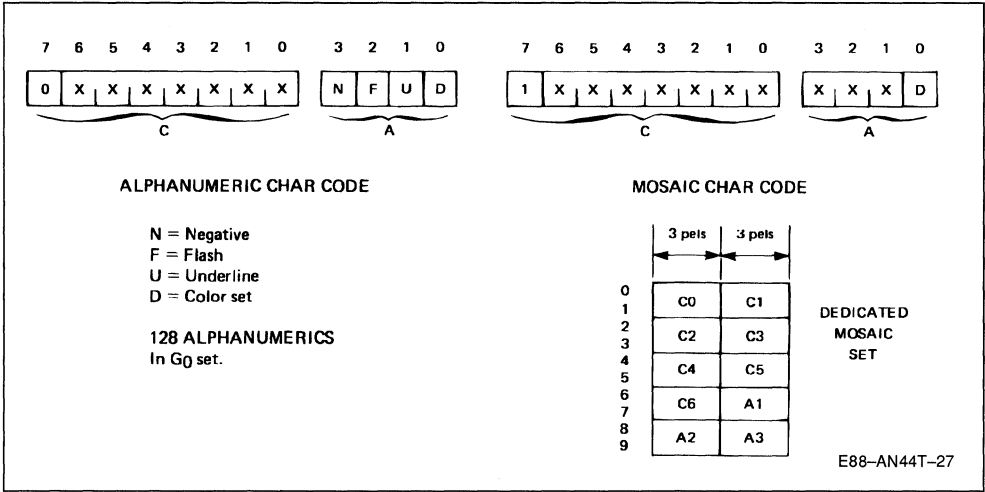








80 Char/Row Character Code









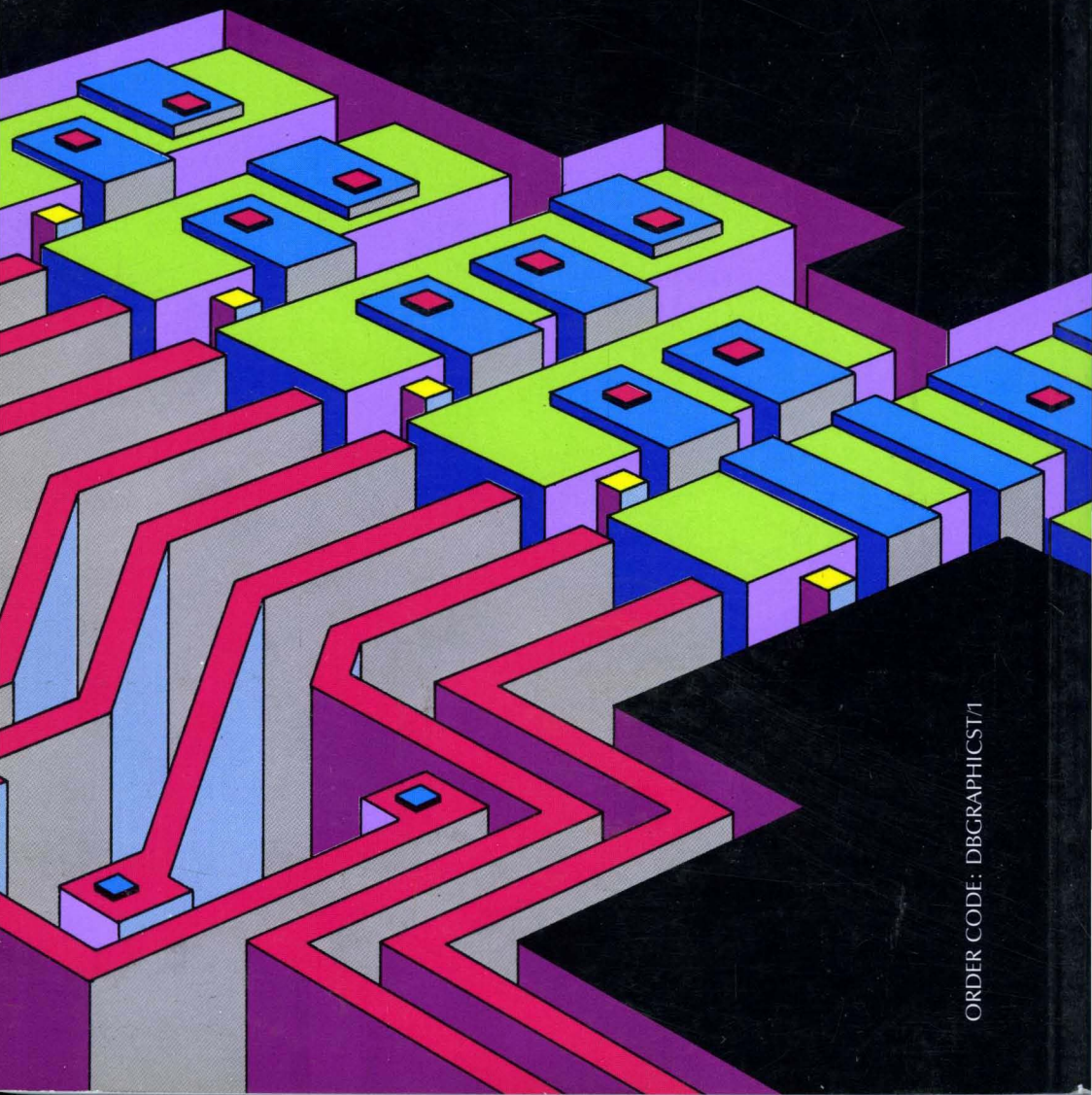
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